IC for System Reset (with built-in watchdog timer)
Monolithic IC MM1099

March 31, 2004

Outline

This IC functions in a variety of CPU systems and other logic systems to generate a reset signal and reset the system accurately when the power is turned on or interrupted.
It includes a watchdog timer which allows diagnosis of the system operation, so that it prevents system runaway by intermittently generating a reset pulse when system misoperation occurs.

Features

1. Built-in watch dog timer
2. Low current consumption — 130μA typ.
3. Low operating threshold voltage — V_{CC}=0.8V
4. Watch dog stop function (RCT pin) included
5. Long clock monitoring time
   T_{PR} (POWER ON) : T_{WD} (clock monitoring)=1 : 1
6. Fewer outer components

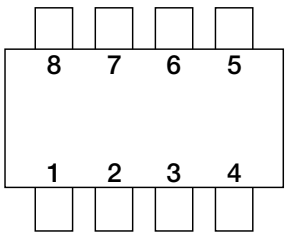
Packages

DIP-8B (MM1099AD, MM1099BD)
SOP-8C (MM1099AF, MM1099BF)

Applications

1. Reset circuits for microcomputers, CPUs and MPUs
2. Reset circuits for logic circuits
3. Microcomputer system monitoring, etc.

Pin Assignmemt



SOP-8C/DIP-8B
(TOP VIEW)

1	TC
2	N.C
3	CK
4	GND
5	V_{CC}
6	RCT
7	V_S
8	$\overline{RESET}$

Pin Description

Pin No.	Pin name	Function
1	TC	Variable terminals T_{WD}, T_{WR} and T_{PR} The time for T_{WD}, T_{WR} and T_{PR} to be determined by the external capacitor. T_{PR} (ms) = 5000×C_T (μF) T_{WD} (ms) = 5000×C_T (μF) T_{WR}(ms) = 100×C_T (μF)
2	N.C	
3	CK	Clock input pin Inputs the clock from the logic system.
4	GND	GND pin
5	V_{CC}	Voltage detection MM1099A→3.2V MM1099B→4.2V
6	RCT	Watchdog timer stop pin Operation modes: Operation→OPEN, Stop→connect to GND
7	V_S	Detect voltage variable pin
8	RESET	Reset output pin (low output)

Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{CC} max.	−0.3~+10	V
CK pin input voltage	V_{CK}	−0.3~V_{CC}+0.3 (≦+10)	V
V_S pin input voltage	V_{VS}	−0.3~V_{CC}+0.3 (≦+10)	V
Voltage applied to RCT pin	V_{RCT}	−0.3~V_{CC}+0.3 (≦+10)	V
Voltage applied to $\overline{\text{RESET}}$ pin	V_{OH}	−0.3~V_{CC}+0.3 (≦+10)	V
Allowable loss	Pd	300	mW
Storage temperature	T_{STG}	−40~+125	℃

Recommended Operating Conditions

Item	Symbol	Rating	Units
Supply Voltage	V_{CC}	+2.2~+7.0	V
$\overline{\text{RESET}}$ Sink Current	I_{OL}	0~1.0	mA
Watchdog Time Monitoring Time Set value	T_{WD}	0.1~5000	ms
Reset Hold Time at Power Rise Set value	T_{PR}	0.1~5000	ms
Clock Rise and Fall Time	t_{RC}, t_{FC}	<100	μs
Operating Temperature	T_{OP}	−25~+75	℃

Electrical Characteristics (DC) (Except where noted otherwise, MM1099A : V_{CC}=3.6V, Ta=25℃, MM1099B : V_{CC}=5.0V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	MM1099A	I_{CC}	During watchdog timer operation		(100)	(150)	μA
	MM1099B				130	195	
Detection voltage	MM1099A	V_{SL}	V_S=OPEN, V_{CC}	3.10	3.20	3.30	V
	MM1099B			4.05	4.20	4.35	
	MM1099A	V_{SH}	V_S=OPEN, V_{CC}	3.15	3.25	3.35	
	MM1099B			4.15	4.30	4.45	
Detection voltage temperature coefficient		$V_S/\Delta T$			±0.01		%/℃
Hysteresis voltage	MM1099A	V_{HYS}	V_{SH}–V_{SL}, V_{CC}	25	50	100	mV
	MM1099B			50	100	150	
CK input threshold		V_{TH}		0.8	1.2	2	V
CK input current		I_{IH}	A : V_{CK}=3.6V, B : V_{CK}=5.0V		0	1	μA
		I_{IL}	V_{CK}=0V	–12	–6	–2	
Output voltage (High)	MM1099A	V_{OH}	$I_{\overline{RESET}}$ =–1μA, V_S=OPEN	3.0	3.4		V
	MM1099B			4.0	4.5		
Output voltage (Low)		$V_{OL}1$	$I_{\overline{RESET}}$ =0.5mA, V_S=0V		0.2	0.4	V
		$V_{OL}2$	$I_{\overline{RESET}}$ =1.0mA, V_S=0V		0.3	0.5	
R output sync current		I_{OL}	$V_{\overline{RESET}}$ =1.0V, V_S=0V	1	2		mA
C_T charge current		$I_{CT}1$	V_{TC}=1.0V during watchdog timer operation	–0.16	–0.24	–0.48	μA
		$I_{CT}2$	V_{TC}=1.0V during power ON reset operation	–0.16	–0.24	–0.48	μA
Minimum operating power supply voltage to ensure $\overline{RESET}$		V_{CCL}	$V_{\overline{RESET}}$ =0.4V $I_{\overline{RESET}}$ =0.1mA		0.8	1.0	V

Electrical Characteristics (AC)

(Except where noted otherwise, MM1096A : V_{CC}=3.6V, Ta=25℃ MM1096B : V_{CC}=5.0V)
(Except where noted otherwise, resistance unit is Ω)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{CC} input pulse width	MM1099A	T_{PI}	V_{CC} 3.6V / 2.8V	8			μs
	MM1099B		V_{CC} 5.0V / 4.0V	8			
CK input pulse width		T_{CKW}	CK or	3			μs
CK input cycle		T_{CK}		20			μs
Watchdog timer monitoring time *1		T_{WD}	C_T=0.02μF	50	100	150	ms
Reset time for watchdog timer *2		T_{WR}	C_T=0.02μF	1	2	3	ms
Reset hold time for power supply rise *3		T_{PR}	C_T=0.02μF, V_{CC}	50	100	150	ms
Output delay time from V_{CC} *4		T_{PD}	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2	10	μs
Output rise time *5		t_R	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2.0	4.0	μs
Output fall time *5		t_F	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		0.2	1.0	μs

Notes :

*1 The "monitoring time" means the time interval from the last pulse of the clock pulses for timer clear (negative edge) to the output of the reset pulse. If the clock pulse is not input during this time interval, the reset output will be given.

*2 The "reset time" is no other than the reset pulse width, except when resetting the POWER ON.

*3 The "reset hold time" is the time interval from the time point when V_{CC} exceeds the detect (V_{SH}) at the time of Power On Reset (Power variation reset) to the reset release ($\overline{RESET}$ output "HIGH").

*4 The "output delay time" means the time interval from when the supply voltage comes lower than the detect voltage (V_{SL}) to when comes the reset state ($\overline{RESET}$ output "Low").

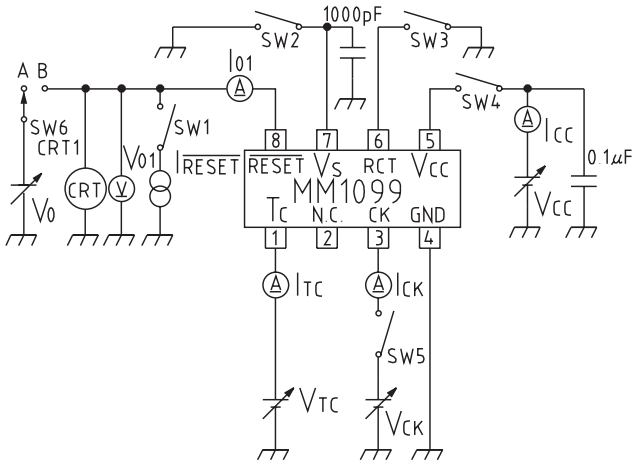
*5 The voltage range is 10 to 90% when measuring the output rise and fall times.

*6 By varying the capacitance of C_T, we can vary the watch dog timer monitoring time (T_{WD}), the reset time at the time of the watch dog timer (T_{WR}), and the reset hold time at the time of power source rise (T_{PR}). The variable time can be expressed by the following formulas:

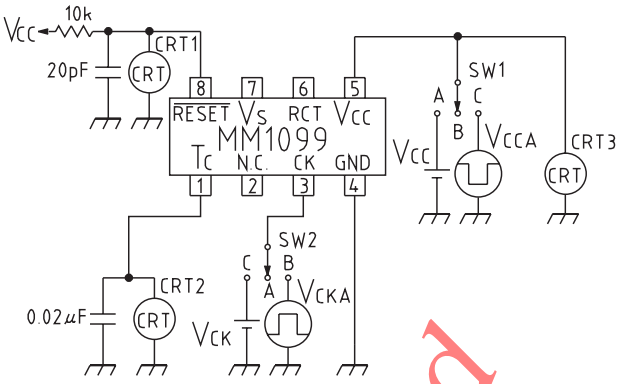
T_{PR} (ms) ≒ 5000 × C_T (μF)
T_{WD} (ms) ≒ 5000 × C_T (μF)
T_{WR} (ms) ≒ 100 × C_T (μF)
Example : When CT=0.02μF
T_{PR} ≒ 100ms
T_{WD} ≒ 100ms
T_{WR} ≒ 2ms

Measuring Circuits

Measuring Circuit 1 (DC)



Measuring Circuit 2 (AC)



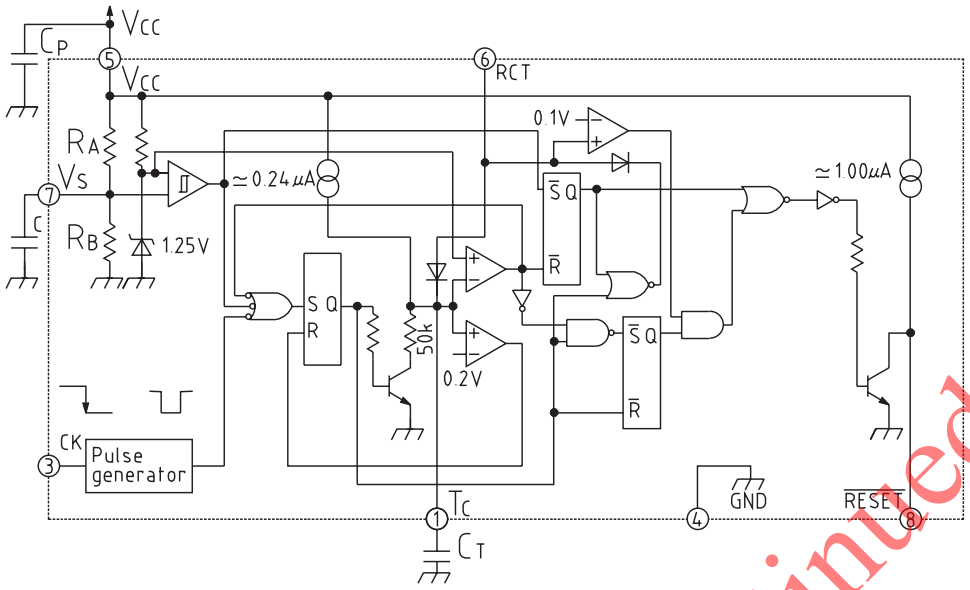
Measuring Circuit 1 SW & Power Supply Table

Item	Symbol	SW1	SW2	SW3	SW4	SW5	SW6	SW7	V_{CC}	V_{CK}	V_{CT}	$I_{\overline{RESET}}$	VM, IM	Notes
Consumption current	I_{CC}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	3.6V	0V	–	I_{CC}	
Detection voltage	V_{SL}	OFF	OFF	ON	ON	ON	ON	A	3.6V→3V	0V	2V	–	V_{O1}, CRT1	
	V_{SH}	OFF	OFF	ON	ON	ON	ON	A	3V→3.6V	0V	2V	–	V_{O1}, CRT1	
CK input threshold	V_{TH}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	0V→3V	1V	–	I_{CK}, V_{CK}	
CK input current	I_{IH}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	3.6V	0V	–	I_{CK}	
	I_{IL}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	0V	0V	–	I_{CK}	
Output voltage (High)	V_{OH}	ON	OFF	ON	ON	ON	ON	A	3.6V	3.6V	2V	–1μA	V_{O1}	
Output voltage (Low)	$V_{OL}1$	ON	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	0.5mA	V_{O1}	
	$V_{OL}2$	ON	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	1.0mA	V_{O1}	
Output sink current	$I_{OL}1$	OFF	ON	ON	ON	ON	ON	B	3.6V	3.6V	2V	–	I_{O1}	V_O=1V
CT charge current 1	$I_{TC}1$	OFF	OFF	OFF	ON	ON	OFF	A	3.6V	–	1V	–	I_{TC}	
CT charge current 2	$I_{TC}2$	OFF	OFF	OFF	ON	ON	OFF	A	3.6V	–	IV	–	I_{TC}	
Minimum operating power supply voltage to ensure $\overline{RESET}$	V_{CCL}	ON	OFF	ON	ON	ON	ON	A	0V→2V	0V	0V	–	V_{O1}, V_{CC}	

Measuring Circuit 2 SW & Power Supply Table

Item	Symbol	SW1	SW2	V_{CCA}	V_{CC}	V_{CKA}	V_{CK}	CRT	Notes
V_{CC} input pulse width	$T_{P}1$	C	B	3.6V / 2.8V, T1	–	1.4V / 0V, T2, T3	–	CRT1 CRT2	T1=8μs
CK input pulse width	T_{CKW}	A	B	–	3.6V	1.4V / 0V, T2 or T2	–	CRT1 CRT2	T2=3μs
CK input cycle	T_{CK}	A	B	–	3.6V	1.4V / 0V, T2, T3	–	CRT1 CRT2	T3=20μs
Watchdog timer monitoring time	T_{WD}	A	A	–	3.6V	–	3.6V	CRT1 CRT2	
Reset time for watchdog timer	T_{WR}	A	A	–	3.6V	–	3.6V	CRT1 CRT2	
Reset hold time for power supply rise	T_{PR}	B→A	A	–	3.6V	–	3.6V	CRT1 CRT2	
Output delay time from V_{CC}	T_{PD}	C	A	3.6V / 0V	–	–	0V	CRT1	
Output rise time	T_R	A	A	–	3.6V	–	3.6V	CRT1	
Output fall time	T_F	A	A	–	3.6V	–	3.6V	CRT1	

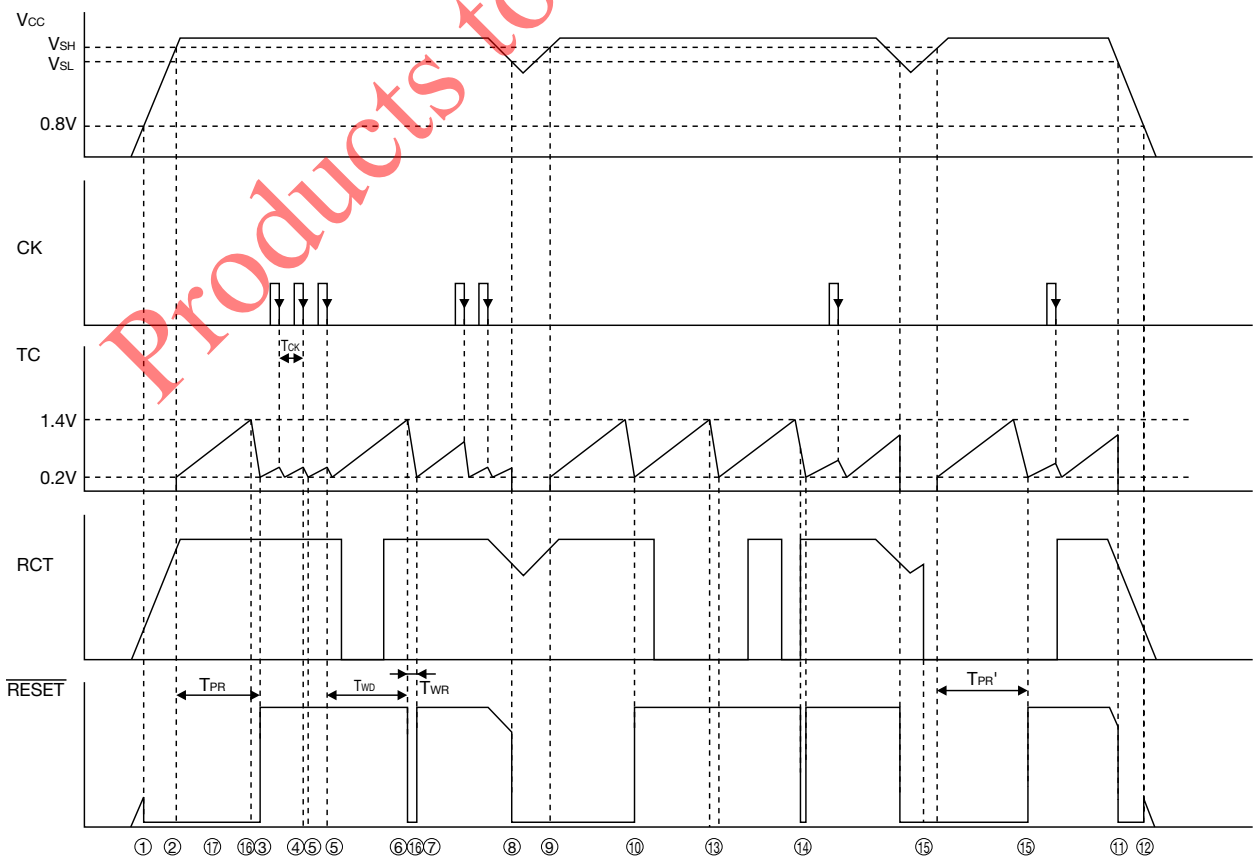
Block Diagram



	RA	RB
MM1099A	≃305k	≃195k
MM1099B	≃350k	≃150k

Note 1. Cp = approx. 0.1μF
Note 2. C ≧ 1000pF
Note 3. The watchdog timer can be stopped by grounding the RCT pin.
(Function as voltage detection circuit.)
Note 4. TPR, TWD can be varied by pulling up the RCT pit to Vcc using a resisteor.

Timing Chart



Description of Operation

1. The $\overline{\text{RESET}}$ will become "Low" if V_{CC} rises to about 0.8V.
   Approximately 1μA (Vcc=0.8V) of pull up current is output from $\overline{\text{RESET}}$
2. Charging starts at the capacitor C_T when V_{CC} riset to V_{SH} (MM1099A ≒ 3.25V, MM1099B ≒ 4.3V), when the output has been reset.
3. The output reset is released after a given interval T_{PR} from when the C_T Starts charging and to when it discharges (that is, the time from when C_T voltage takes a given value 1 (≒ 1.4V) up until decreases to a given value 2 (≒ 0.2V). ($\overline{\text{RESET}}$ will become "High"). The RESET will output a pull up current, about 1μA (V_{CC}=0.8V). The reset hold time T_{PR} is expressed by the following formula:
   T_{PR} (ms) ≒ 5000 × C_T (μF)
   After the reset release C_T restarts charging and the watch dog timer begins operating.
   Note that input of clock while POWER ON RESET time T_{PR} will cause an erroneous operation.
4. If clock is input into CK terminal while C_T is charging (negative edge trigger), C_T changes from charging over to discharging.
5. When the C_T voltage decreases to a given threshold (≒ 0.2V), then discharging changes over to charging. Steps 4 and 5 will be repeated while normal clock is input from the logic system.
6. When the clock ceases and C_T voltage reaches the RESET ON threshold (≒ 1.4V), the output enters into reset state ($\overline{\text{RESET}}$ becoming "Low").
   The C_T charging time T_{WD} up until the reset is output (watch dog monitoring time) is expressed by the following formula:
   T_{WD} (ms) ≒ 5000 × C_T (μF)
7. The reset time at the time of watch dog time T_{WR} is the discharging time while the C_T voltage lowers down to the reset off threshold (≒ 0.2V). The calculation formula:
   T_{WR} (ms) ≒ 100 × C_T (μF)
   After the reset off threshold is reached, the output reset is released and C_T commences to charge. If thenceforth the clock is input normally, steps 4 and 5 will be repeated, and setps 6 and 7 repeated if the clock ceases.
8. When V_{CC} lowers down to V_{SL} (MM1099A ≒ 3.2V, MM1099B ≒ 4.2V), the reset is output. At the same time C_T charged.
9. C_T discharging starts when V_{CC} rises up to V_{SH}.
   If V_{CC} lower instantaneously, charging starts after load discharging of C_T if the time interval from when V_{CC} comes lower than V_{SL} up until when it rises to V_{SH} or higher is equal or superior to the reference value of V_{CC} input pulse width T_{PI}.
10. The output reset is released T_{PR} after V_{CC} becomes V_{SH} or higher, and the watch dog time will start. Then if V_{CC} becomes V_{SL} or lower, steps 8 to 10 will be repeated.
11. If power Off occurs, reset is output if V_{CC} becomes V_{SL} or lower.
12. When V_{CC} comes down to 0V, the reset output will hold up until V_{CC} becomes 0.8V.
13. Output of the reset pulse stops if RCT pin goes "LOW".
14. TC pin keeps charging/discharging even if RCT pin goes "LOW". Therefore if RCT is release and C_T is discharged at the same time, output goes "LOW" when RCT release. To avoid this operation, input CK before the TWR time of RCT release and discharge C_T.
15. When started up with the RCT pin at "LOW," reset output is cancelled after power ON time elapses. (It operates as if for power ON reset.) The power ON reset time is the same time as T_{WD}.
    T_{PR}' ≒ T_{WD} ≒ 4900 × C_T (μF)
16. During power ON reset and watchdog timer, a spike may appear in the output at the point where C_T switches from charge to discharge. When this reset output spike causes operational problems, add a COUT capacitor between $\overline{\text{RESET}}$ and GND. The recommended value is as follows.
    C_{OUT} (μF) > 10^4 × C_T (μF)/R_L (Ω)
17. $\overline{\text{RESET}}$ output keeps "LOW" if CK is input during T_{PR}. $\overline{\text{RESET}}$ output goes "HIGH" once CK is released. Noise jumps into CK easily if CK output of microcomputer is high impedance during T_{PR}. Pull down a resistance (approx. 10-100kΩ) to CK pin and lower the impedance or keep the IC away from noise if there's a possibility of defects such as $\overline{\text{RESET}}$ output keeps "LOW" due to CK malfunction caused by noise.