# System Reset
# Monolithic IC PST575

## Outline

This IC functions in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted. This ultra-low current consumption low reset type system reset IC has a built-in delay time generating circuit that can set the time by an external capacitor and resistor. It is ideal for use in multi-CPU systems because a fast-rising output waveform can be obtained.

## Features

| | |
|---|---|
| 1. Ultra-low current consumption | $I_{CCH}$=7.5μA typ. $I_{CCL}$=400μA typ. |
| 2. Low operating limit voltage | 0.65V typ. |
| 3. Output current high for ON | 30mA typ. |
| 4. Hysteresis voltage provided in detection voltage | 50mV typ. |
| 5. Delay time can set over a wide range using external capacitor and resistor. | 10μS~10S |
| 6. 10 ranks of detection voltage | PST575 C : 4.5V typ. H : 3.1V typ. |
| | D : 4.2V typ. I : 2.9V typ. |
| | E : 3.9V typ. J : 2.7V typ. |
| | F : 3.6V typ. K : 2.5V typ. |
| | G : 3.3V typ. L : 2.3V typ. |

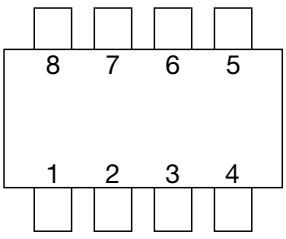
## Package

MMP-4A (PST575□M)
DIP-8A (PST575□)
* □contains detection voltage rank

## Applications

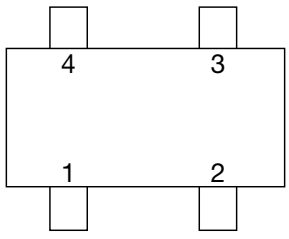
1. Reset circuits in microcomputers, CPUs and MPUs (especially multi-CPU sets)
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.

## Pin Assignment




| | |
|---|---|
| 3 | GND |
| 4 | Cd |
| 5 | $V_{OUT}$ |
| 7 | $V_{CC}$ |

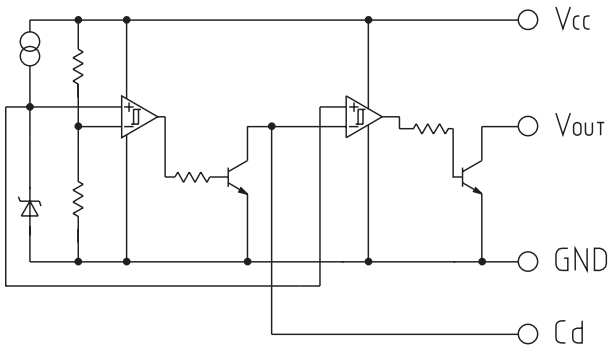
DIP-8A




| | |
|---|---|
| 1 | $V_{CC}$ |
| 2 | $V_{OUT}$ |
| 3 | Cd |
| 4 | GND |

MMP-4A

## Equivalent Circuit Diagram




## Absolute Maximum Ratings (Ta=25℃)

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Storage temperature | Tstg | −40~+125 | ℃ |
| Operating temperature | Topr | −20~+75 | ℃ |
| Power supply voltage | Vcc max. | −0.3~10 | V |
| Allowable loss | Pd | 200 (MMP-3A)<br>300 (TO-92A) | mW |

## Electrical Characteristics (Ta=25℃) (Except where noted otherwise, resistance unit is Ω)

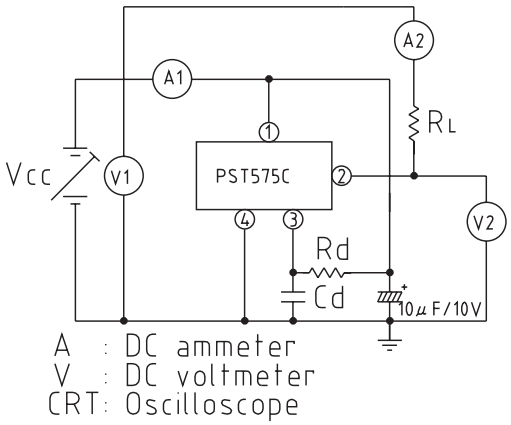
| Item | Symbol | Measuring circuit | Measurement conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| Detection voltage | Vs | 1 | RL=470<br>VOL≦0.4V<br>Vcc=H→L | PST575C | 4.3 | 4.5 | 4.7 | V |
| | | | | PST575D | 4.0 | 4.2 | 4.4 | |
| | | | | PST575E | 3.7 | 3.9 | 4.1 | |
| | | | | PST575F | 3.4 | 3.6 | 3.8 | |
| | | | | PST575G | 3.1 | 3.3 | 3.5 | |
| | | | | PST575H | 2.9 | 3.1 | 3.3 | |
| | | | | PST575I | 2.75 | 2.90 | 3.05 | |
| | | | | PST575J | 2.55 | 2.70 | 2.85 | |
| | | | | PST575K | 2.35 | 2.50 | 2.65 | |
| | | | | PST575L | 2.15 | 2.30 | 2.45 | |
| Hysteresis voltage | ⊿Vs | 1 | RL=470, Vcc=L→H→L | | 25 | 50 | 100 | mV |
| Detection voltage temperature coefficient | Vs/⊿T | 1 | RL=470, Ta=−20℃~+75℃ | | | ±0.01 | | %/℃ |
| Low-level output voltage | VOL | 1 | Vcc=Vs min.−0.05V, RL=470 | | | 0.1 | 0.4 | V |
| Output leakage current | IOH | 1 | Vcc=7.5V | | | | ±0.1 | μA |
| Circuit current while on | ICCL | 1 | Vcc=Vs min.−0.05V, RL=∞ | | | 400 | 650 | μA |
| Circuit current while off | ICCH | 1 | Vcc=Vs typ./0.85V, RL=∞ | | | 7.5 | 12.0 | μA |
| "H" transport delay time | tpLH | 2 | Rd=100k, Cd=0.01μF ✶1 | | 0.75 | 1.25 | 1.75 | mS |
| "L" transport delay time | tpHL | 2 | Rd=100k, Cd=0.01μF ✶1 | | | 6 | 20 | μS |
| Operating power supply voltage | VopL | 1 | RL=4.7kΩ, VOL ≦ 0.4V | | | 0.65 | 0.85 | V |
| Output current while on Ⅰ | IOL Ⅰ | 1 | Vcc=Vs min.−0.05V, RL=0 | | 8 | 30 | | mA |
| Output current while on Ⅱ | IOL Ⅱ | 1 | Ta=−20℃~+75℃, RL=0 ✶2 | | 5 | | | mA |
| Threshold voltage for delay time setting comparator (CO2) | Vtsh | 1 | Vcc=5.0V, Rd=100k, Cd=0.01μF<br>RL=4.7k, CL=100pF | | 3.5 | 3.7 | 3.9 | V |

*1 : tpLH : Vcc= (Vs typ.−0.4V) → (Vs typ.+0.4V), tpHL : Vcc= (Vs typ.+0.4V) → (Vs typ.−0.4V), CL=100pF

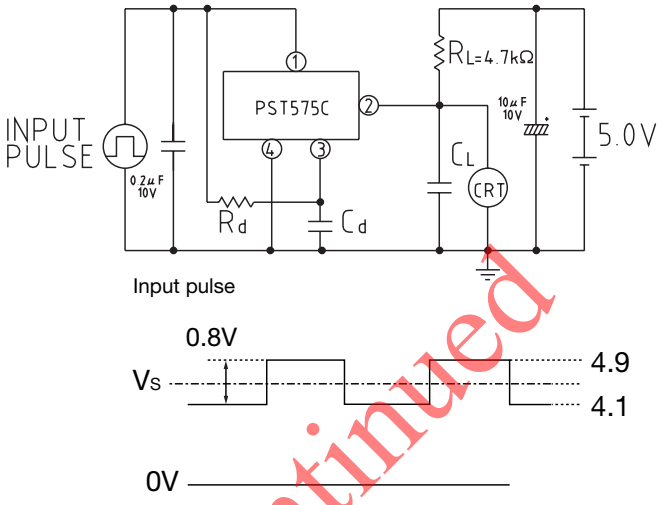
*2: Vcc=Vs min.−0.15V

## Measuring Circuit (Example: PST575C)

[1]



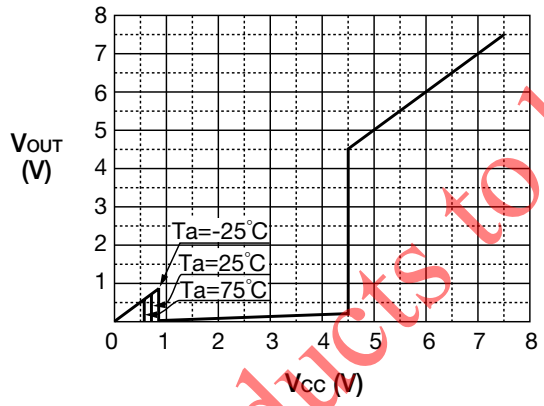

[2]



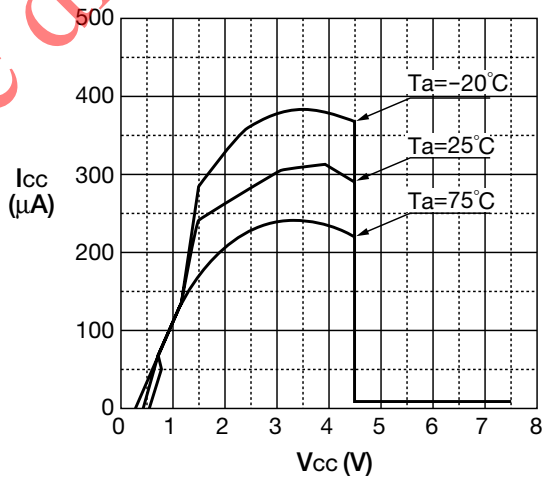

Note: Input model is an example for PST575C (MMP-4P).

## Characteristics (Example: PST575C)

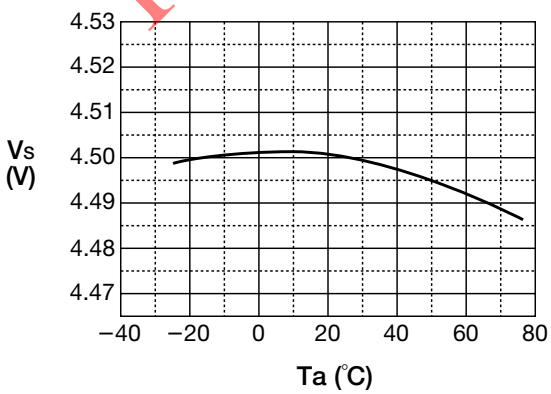
### VCC vs. VOUT



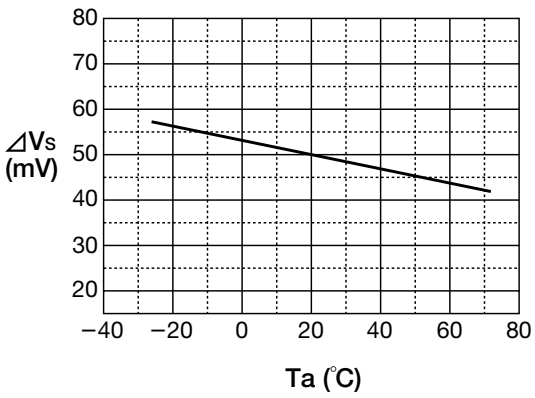

### VCC vs. ICC



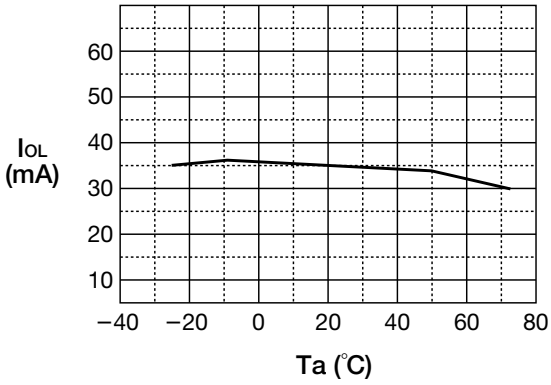

### VS vs. Ta



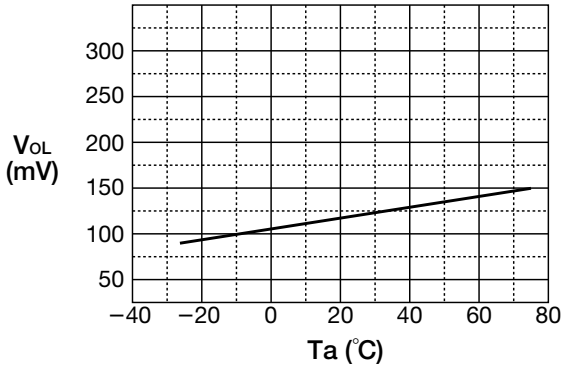

### ⊿VS vs. Ta



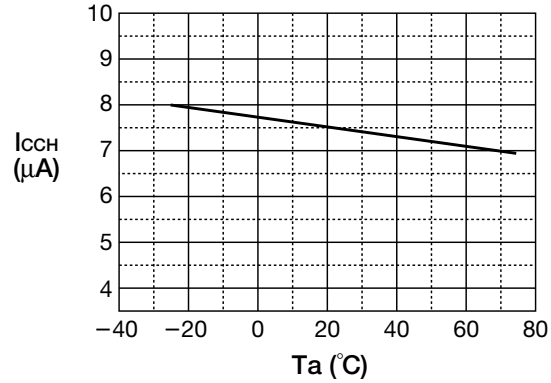
## IOL vs. Ta



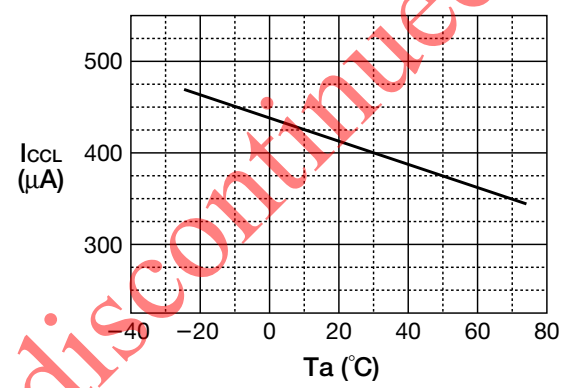

## VOL vs. Ta



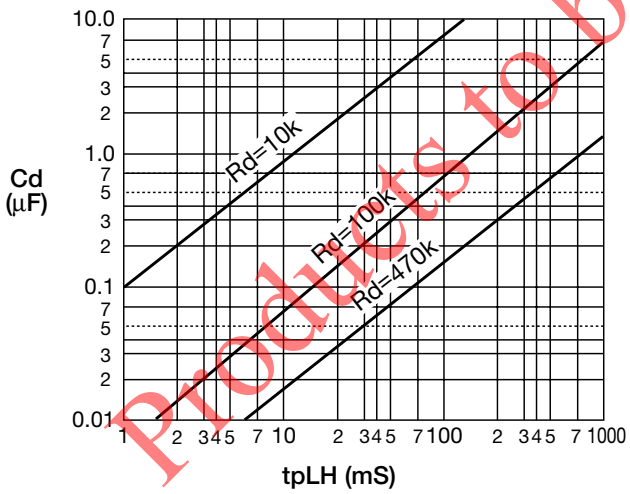

## ICCH vs. Ta



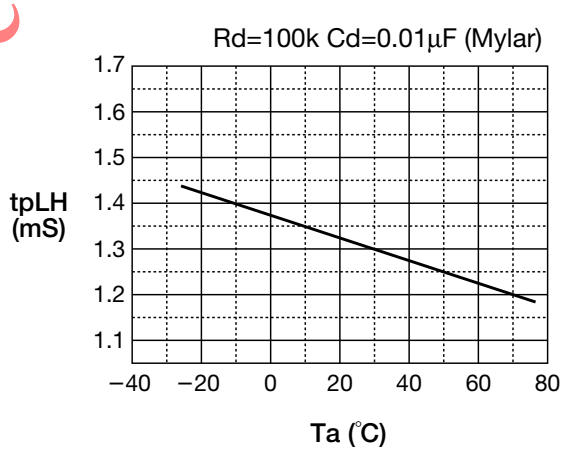

## ICCL vs. Ta



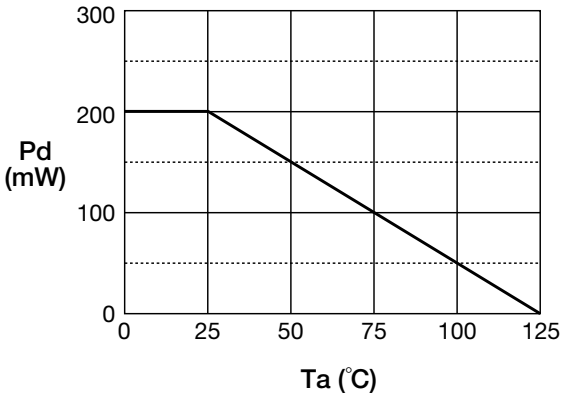

## Cd (Rd) vs. tpLH



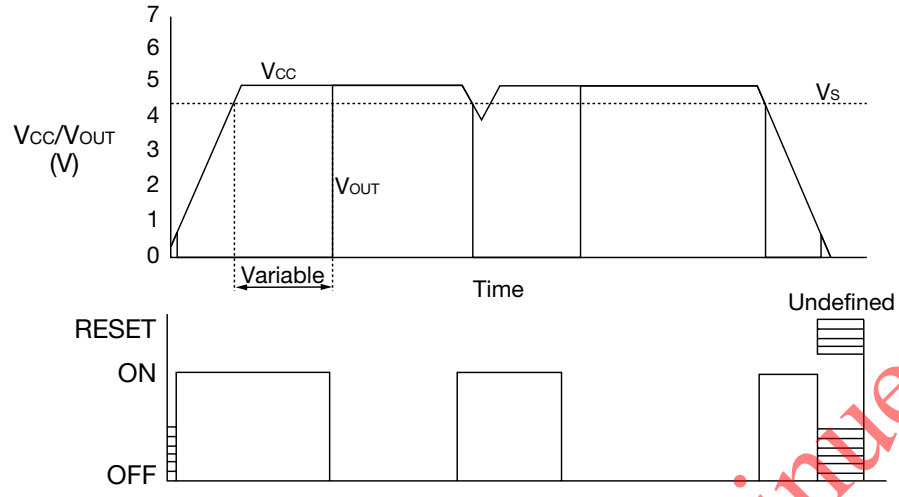

## tpLH vs. Ta




## Pd vs. Ta

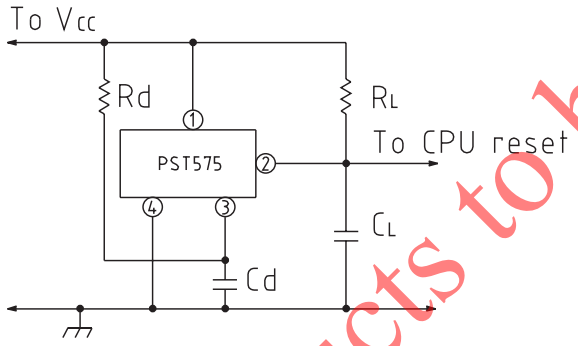


## Timing Chart



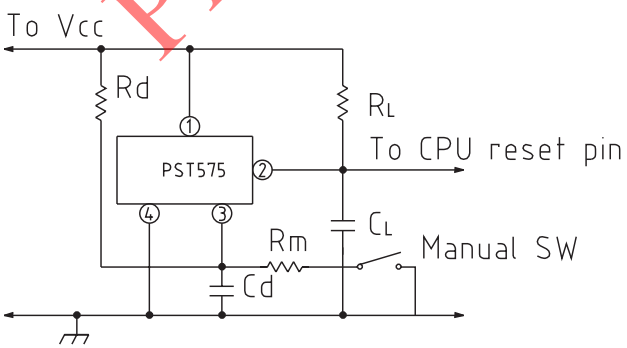

## Application Circuits (Pin numbers are for an example of MMP-4P.)

**1. Normal hard reset**



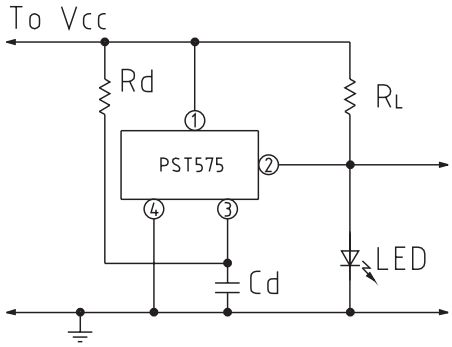

Delay time (tPLH)
≒1.3Cd×Rd+0.007 (mS)
Cd : μF Rd : kΩ
Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

**2. Manual reset added**



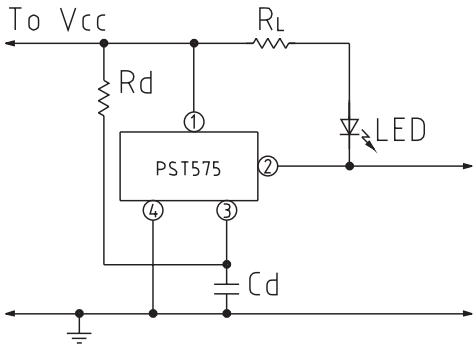

Note: Use RL, CL and Rm to prevent manual switch chattering. Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

### 3. Battery checker (LED ON for high voltage)



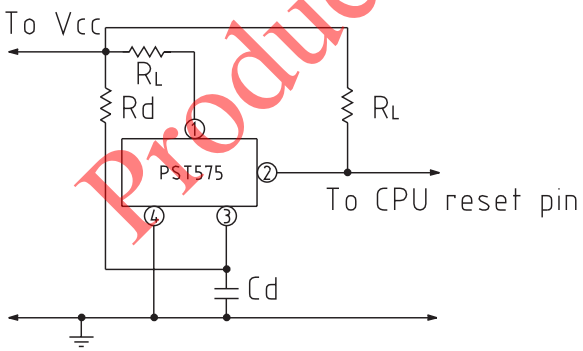

Note: Connect a capacitor between IC pins 1 and 2 if $V_{CC}$ line impedance is high.

### 4. Battery checker (LED ON for low voltage)




Note: Connect a capacitor between IC pins 1 and 2 if $V_{CC}$ line impedance is high.

### 5. Hysteresis voltage UP method




When increasing hysteresis voltage for stable system operation, determine RH as follows and connect externally.
However, $I_{CCH}$ is −5000PPM/℃, so perform temperature compensation at RH when using over a wide temperature range.
Hysteresis voltage UP amount (⊿Vsup) is
$\Delta V_{sup} \fallingdotseq RH \times I_{CCL}$
Total hysteresis voltage (⊿Vstotal) is
$\Delta V_{stotal} \fallingdotseq Vs + \Delta V_{sup}$
(Operation will be destabilized is RH is raised too much.)

Note: Connect a capacitor between IC pins 1 and 2 if $V_{CC}$ line impedance is high.