I²C Bus Control 13-Input 4-Output Audio Switch
Monolithic IC MM1699XJ

Outline

This IC is an I²C bus controlled audio switch IC for rear projection, PDP, and LCD TVs (medium-end to high-end TVs).
The design of the input select block can be simplified by using with a video switch IC.
It provides stereo or selected mono output.

Features

1. 13 audio signal (L, R) input channels, 4 output channels
2. 4 output channels are independent and can receive any input.
3. High input dynamic range (3Vrms)
4. All the outputs can be switched to stereo/mono.
5. Built-in gain switch (0dB/12dB) * OUT1 only
6. Built-in power save function

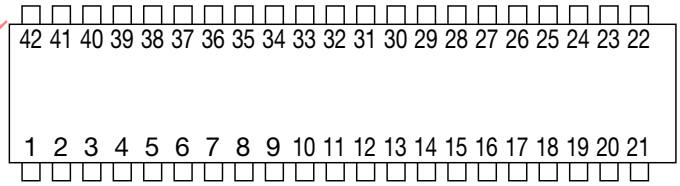
Package

SSOP-42A

Applications

1. Rear projection TVs
2. PDP TVs
3. TVs (medium-end to high-end TVs)
4. CRT TVs

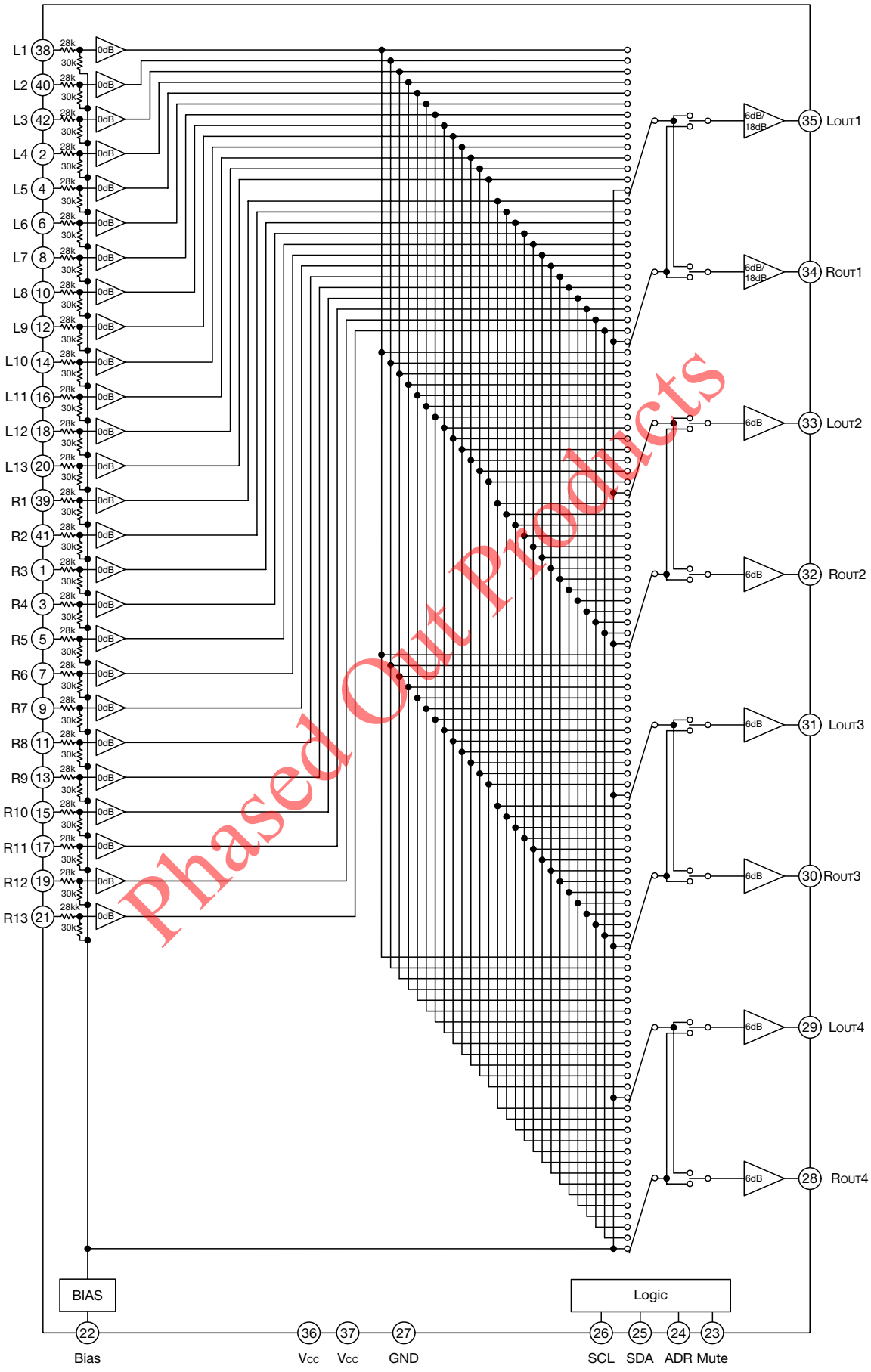
Pin Assignment



SSOP-42
(TOP VIEW)

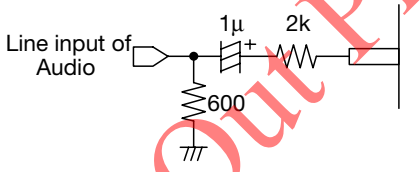
1	R3	8	L7	15	R10	22	BIAS	29	LOUT4	36	VCC
2	L4	9	R7	16	L11	23	MUTE	30	ROUT3	37	VCC
3	R4	10	L8	17	R11	24	ADR	31	LOUT3	38	L1
4	L5	11	R8	18	L12	25	SDA	32	ROUT2	39	R1
5	R5	12	L9	19	R12	26	SCL	33	LOUT2	40	L2
6	L6	13	R9	20	L13	27	GND	34	ROUT1	41	R2
7	R6	14	L10	21	R13	28	ROUT4	35	ROUT1	42	L3

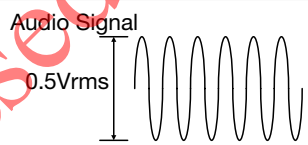
Block Diagram

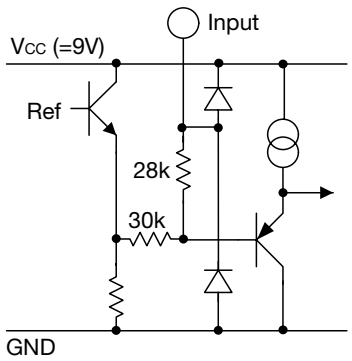


Pin Description

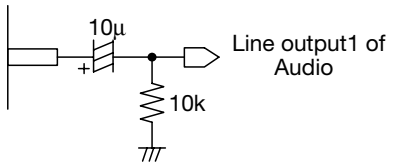
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">1~21
38~42</td><td rowspan="2">L1~L13
R1~R13</td><td>
Function
Audio line input
Pin to input audio signals. It includes 13 channels; L1 - L13, R1 - R13. Voltage gain can be adjusted by changing a constant of an external input resistor.

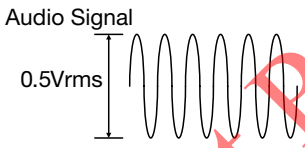
Adjusting voltage gain with an external input resistor
<table>
<tr><th>External input resistor</th><th>Input impedance</th><th>Voltage gain of OUT1</th><th>Voltage gain of OUT2-4</th></tr>
<tr><td>0Ω</td><td>58kΩ</td><td>0.3dB/12.3dB</td><td>0.3dB</td></tr>
<tr><td>2kΩ</td><td>60kΩ</td><td>0dB/12dB</td><td>0dB</td></tr>
<tr><td>3.9kΩ</td><td>61.9kΩ</td><td>–0.3dB/11.7dB</td><td>–0.3dB</td></tr>
<tr><td>5.6kΩ</td><td>63.6kΩ</td><td>–0.5dB/11.5dB</td><td>–0.5dB</td></tr>
</table>
Terminal voltage: 4.50V typ.
Input impedance: 60kΩ typ.
*Input impedance contains an external input resistor of 2kΩ.
Input dynamic range: 3Vrms typ.
External circuit


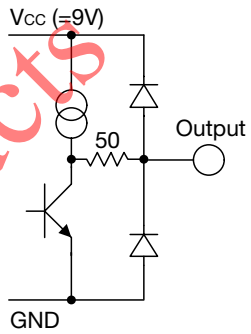
If unused, connect to GND with 1µF.
Input signal


Equivalent circuit diagram


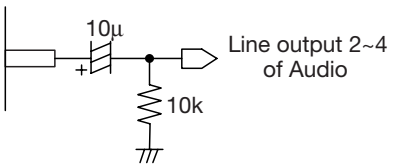
</td></tr>
</table>

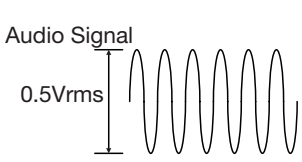
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>34~35</td><td>LOUT1
ROUT1</td><td>
Function
Audio line output 1
Pin to output audio signals
· Select voltage gain 0dB/12dB with control resister, b34.
(b34=0: 0dB mode, b34=1: 12dB mode)
· Select stereo/mono with control registers, b21/b20.
(b21=0 b20=0: stereo, b21=0 b20=1: mono1, b21=1 b20=0: mono2)
Terminal voltage: 4.50V typ.
Voltage gain: 0dB/12dB typ.
Frequency characteristic: –3dB at 50kHz min.
External circuit


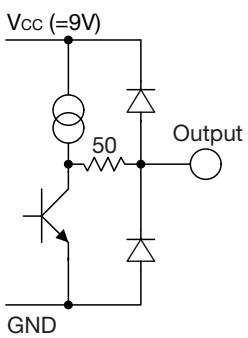
If unused: open
Output signal


Equivalent circuit diagram


</td></tr>
<tr><td>28~33</td><td>LOUT2~4
ROUT2~4</td><td>
Function
Audio line output 2-4
Pin to output audio signals
· Select stereo/mono with control registers b27 - b22.
Audio line output 2 (b23=0 b22=0: stereo, b23=0 b22=1: mono1, b23=1 b22=0: mono2)
Audio line output 3 (b25=0 b24=0: stereo, b25=0 b24=1: mono1, b25=1 b24=0: mono2)
Audio line output 4 (b27=0 b26=0: stereo, b27=0 b26=1: mono1, b27=1 b26=0: mono2)

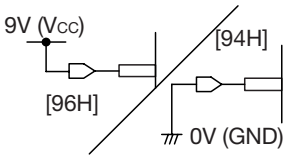
Terminal voltage: 4.50V typ.
Voltage gain: 0dB typ.
Frequency characteristic: –3dB at 50kHz min.
External circuit


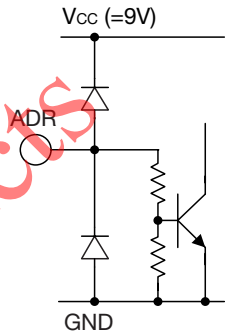
If unused: open
Output signal


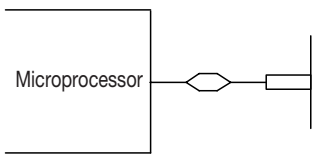
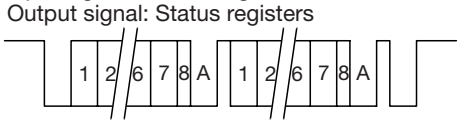
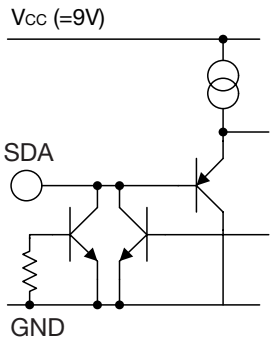
Equivalent circuit diagram


</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">24</td><td rowspan="4">ADR</td><td>Function
Slave address select pin
I²C slave address 94H or 96H can be selected with voltage to be applied to this pin.
Set ADR pin to "L" for address 94H and "H" for 96H.

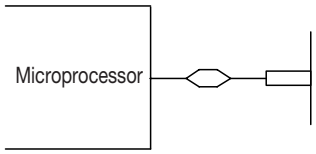
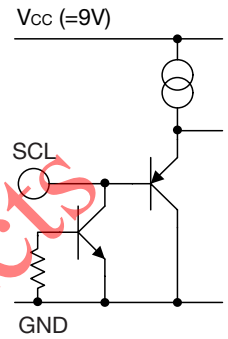
Threshold: 2.0V typ.
Input impedance: 100kΩ typ.</td></tr>
<tr><td>External circuit
 

If unused: open</td></tr>
<tr><td>Input signal
DC voltage:
0V (GND) or 9V (Vcc)</td></tr>
<tr><td>Equivalent circuit diagram
 
</td></tr>
<tr><td rowspan="4">25</td><td rowspan="4">SDA</td><td>Function
Data input of I²C BUS
I/O pin for data signal of I²C BUS

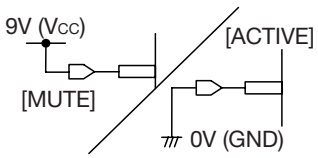
Threshold: 2.1V typ.</td></tr>
<tr><td>External circuit
 
</td></tr>
<tr><td>Input signal
Input signal: Control registers
Output signal: Status registers
 
</td></tr>
<tr><td>Equivalent circuit diagram
 
</td></tr>
</table>

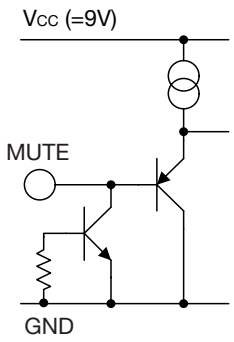
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">26</td><td rowspan="4">SCL</td><td colspan="2">Function

CLK input of I²C BUS
I/O pin for clock signal of I²C BUS

Threshold: 2.1V typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 
</td><td rowspan="2"> 
</td></tr>
<tr><td>Input signal
 
</td></tr>
<tr><td rowspan="4">23</td><td rowspan="4">MUTE</td><td colspan="2">Function

Mute select pin
Output can be selected mute/active by applying voltage to this pin.
Set MUTE pin to "H" for mute and "L" for active.
When MUTE pin is set to "H", all the audio output pins are connected to internal bias
voltage. When Mute level returns from "H" to "L", audio output select returns to the previous condition.

Threshold: 2.1V typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

If unused: GND</td><td rowspan="2"> 
</td></tr>
<tr><td>Input signal

DC voltage:
0V (GND) or 9V (Vcc)</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">22</td><td rowspan="4">BIAS</td><td>Function</td></tr>
<tr><td>BIAS
All the reference voltages used inside the IC are generated based on the resistance divider of this pin. It is the pin which connects a filter capacitor for criteria voltage stabilization.

Input impedance: 12.5kΩ typ.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>22µ
If unused, connect to GND with 22µF.
Input signal

Vcc (=9V) 25k BIAS 25k GND</td></tr>
<tr><td rowspan="4">36
37</td><td rowspan="4">Vcc</td><td>Function</td></tr>
<tr><td>Voltage supply
Pin to apply supply voltage. Apply 9V.
36pin and 37pin are shorted inside the IC.
Note: Place a bypass capacitor as close to the pin as possible.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>Vcc=9V 100µ 0.1µ
Input signal
DC voltage:
+8.0~+10.0V</td></tr>
<tr><td rowspan="2">27</td><td rowspan="2">GND</td><td>Function</td></tr>
<tr><td>GND pin</td></tr>
</table>

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−65~+150	°C
Operating temperature	T_{OPR}	−40~+85	°C
Supply voltage	$V_{CC\ max.}$	−0.2~+13	V
I/O terminal voltage	$V_{IN\ max.}$, $V_{OUT\ max.}$	−0.2~V_{CC}+0.2	V
Output current	$I_{OUT\ max.}$	25	mA
Junction temperature	$T_{j\ max.}$	150	°C
Allowable loss (Note1)	Pd	2.4	W

Note1: Power dissipation when mounted on a board. Board size 190mm×150mm×1.6mm

Recommended Operating Conditions

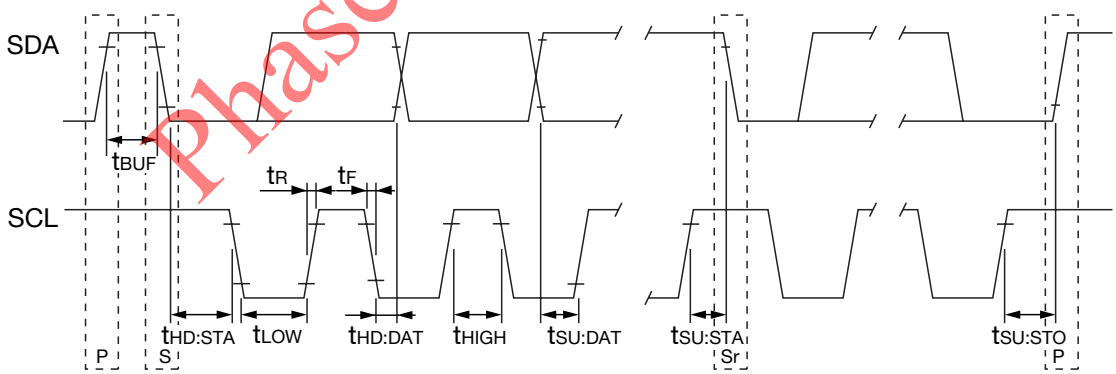
Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	−40~+85	°C
Operating voltage	V_{CCOP}	+8.0~+10.0	V
Operating I/O voltage	V_{INOP}, V_{OUTOP}	0~V_{CC}	V

Electrical Characteristics (Except where noted otherwise Ta=25°C, V_{CC}=9V, SW1 ON, SW2 OFF, SW3 ON)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption		I_{CC0}	No signal, No load		42	55	mA
Current consumption 1 in power save mode		I_{CC1}	Out1 (or Out2 or Out3 or Out4) : power-save Out2 & Out3 & Out4 (or Out1 & Out3 & Out4 or Out1 & Out2 & Out4 or Out1 & Out2 & Out3) : active		37	49	mA
Current consumption 2 in power save mode		I_{CC2}	Out1 & Out2 (or Out1 & Out3 or Out1 & Out4 or Out2 & Out3 or Out2 & Out4 or Out3 & Out4) : power-save Out3&Out4 (or Out2 & Out4 or Out2 & Out3 or Out1 & Out4 or Out1 & Out3 or Out1 & Out2) : active		32	42	mA
Current consumption 3 in power save mode		I_{CC3}	Out1 & Out2 & Out3 (or Out1 & Out2 & Out4 or Out1 & Out2 & Out4 or Out2 & Out3 & Out4) : power-save Out4 (or Out3 or Out2 or Out1) : active		27	36	mA
Current consumption 4 in power save mode		I_{CC4}	Out1 & 2 & Out3 & Out4: power-save		22	30	mA
Voltage gain	0dB	Gv1	SG: 1Vrms, 1kHz	−0.5	0	0.5	dB
	12dB	Gv2	SG: 0.25Vrms, 1kHz	11.4	12.0	12.6	
Frequency characteristic	0dB	FBW1	SG: 1Vrms, 50kHz/1kHz	−3			dB
	12dB	FBW2	SG: 0.25Vrms, 50kHz/1kHz				
Total harmonic distortion		THD	SG: 1Vrms, 1kHz, Gv=0dB		0.03	0.05	%
Input dynamic range		DR	f=1kHz, THD=0.5%, Gv=0dB	2.8	3.0		Vrms
Crosstalk		CT	SG: 1Vrms, f=1kHz Without power save mode		−90	−80	dB
Ripple rejection ratio		PSRR	Vr: 100mVrms, 100Hz, Gv=0dB SW1 OFF, SW2 ON, SW3 OFF		−50	−40	dB
Output offset voltage	0dB	V_{OFF1}	V_{OUT} (Active)−V_{OUT} (Mute)	−15	0	15	mV
	12dB	V_{OFF2}		−60	0	60	
S/N ratio	OUT1, 2, 3, 4	S/N1	SG: 1Vrms, 1kHz, Gv=0dB, A curve		−90	−80	dB
	OUT1	S/N2	SG: 0.25Vrms, 1kHz, Gv=12dB, A curve		−80	−70	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input impedance of input terminals	Z_{IN}	Including an external input resistor of 2kΩ	47	60	73	kΩ
Input terminal voltage	V_{IN}	No signal, No load	4.25	4.50	4.75	V
Output terminal voltage	V_{OUT}	No signal, No load	4.25	4.50	4.75	V
Audio signal input voltage (SG1~22)	V_{SG}	No output signal turnup			7.1	Vrms
MUTE input voltage L	V_{MUIL}	Out: Active	0.0		0.8	V
MUTE input voltage H	V_{MUIH}	Out: Mute	2.5		9.0	V
ADR input voltage L	V_{ADRL}	94H select	0.0		0.8	V
ADR input voltage H	V_{ADRH}	96H select	2.5		9.0	V
[I²C conditions]						
Input voltage L	V_{IL}		0.0		0.8	V
Input voltage H	V_{IH}		2.2		5.0	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
Start condition setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		0			µs
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA, SCL rise time	t_R				1000	ns
SDA, SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			µs

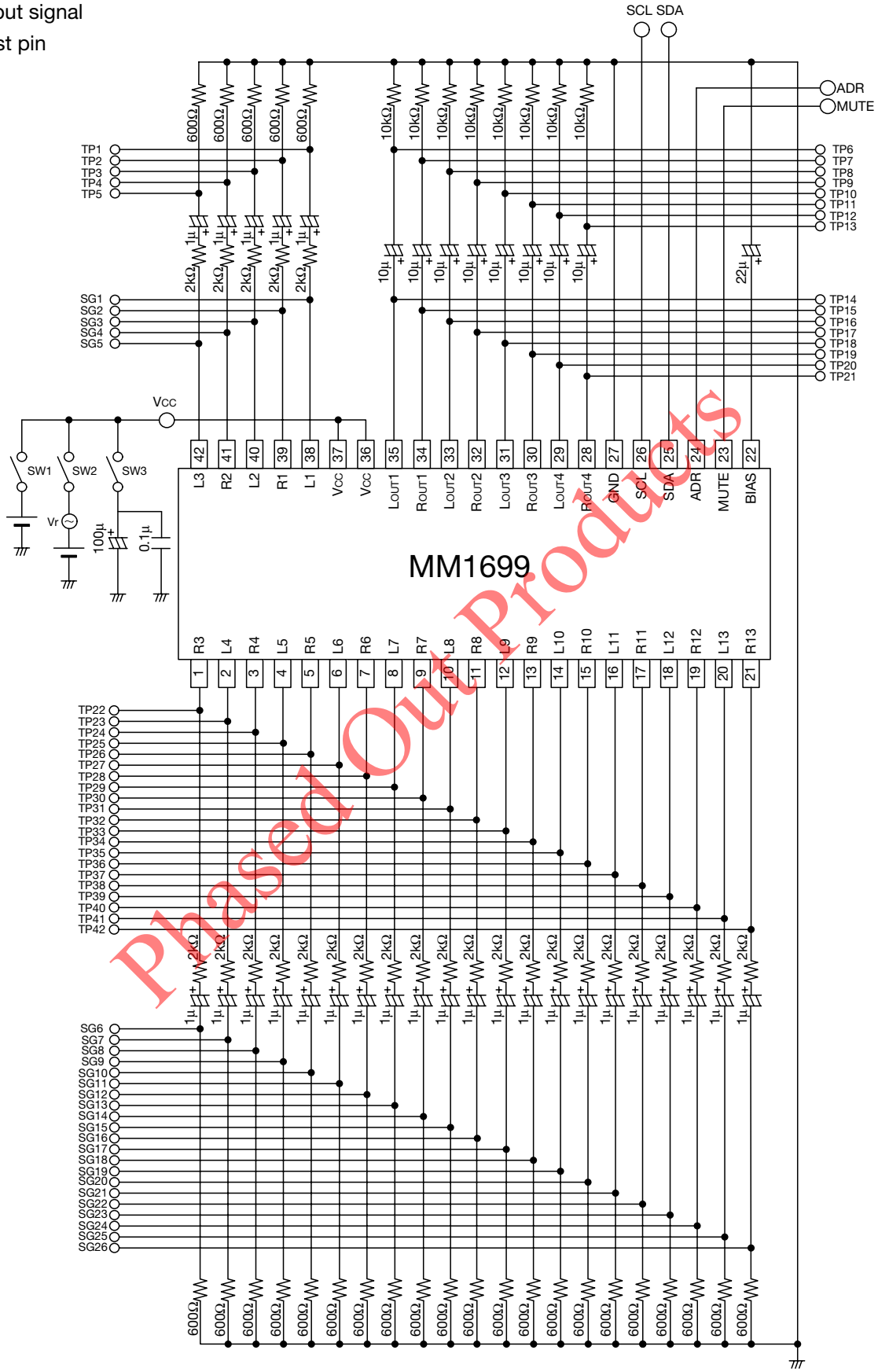
I²C condition



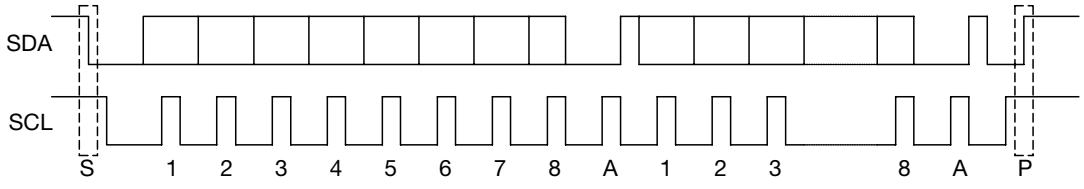
Measuring Circuit

SG: Input signal

TP: Test pin

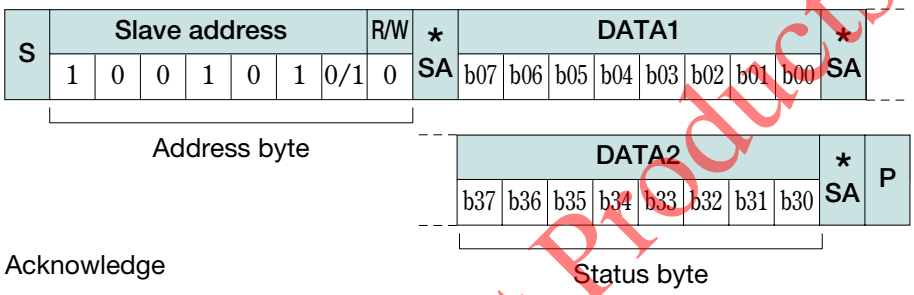


I²C BUS



I²C BUS is inter-IC BUS system to transfer data by 2 lines of SDA and SCL.
Data transfer is performed by 1 byte, and acknowledgment is sent when each byte is complete. Data transfer takes place MSB first from the Start condition.

[Control registers]
Control registers are data transmitted from the master to determine the status of MM1699 (switch) . The data format is set as shown in the figure below.



*SA: Slave Acknowledge

The first 7 bits of the address byte are assigned to the slave address, and the remaining 1 bit to the R/W bit.
To use as control registers, set 0 to the R/W bit.
In addition, MM1699 allows users to select address 94H or 96H according to the ADR pin condition. When ADR pin is set to "L", address 94H is selected.
The following table shows the relation between each bit of control registers and switch control.
Each bit of control registers is reset to 0 during power-up.

MM1699 consists of 1 address byte and 4 control data bytes, 5 bytes in total to control switches. All the prolonged data (after the 6th byte) are ignored.
Refer to the attached switch control table for details.

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	L2, R2 LINE SELECT				L1, R1 LINE SELECT			
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
	L4, R4 LINE SELECT				L3, R3 LINE SELECT			
DATA3 [00H]	b27	b26	b25	b24	b23	b22	b21	b20
	OUT SELECT (out4)		OUT SELECT (out3)		OUT SELECT (out2)		OUT SELECT (out1)	
DATA4 [00H]	b37	b36	b35	b34	b33	b32	b31	b30
				GAIN SW (out1)	Power Save (out4)	Power Save (out3)	Power Save (out2)	Power Save (out1)

*[00H] is in the initial state of control registers.

Switch control table

L1, R1 Line select

b03	b02	b01	b00	L1, R1OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
1	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	L12, R12
1	1	0	1	L13, R13
1	1	1	0	Mute
1	1	1	1	Mute

L2, R2 Line select

b07	b06	b05	b04	L2, R2OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
1	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	L12, R12
1	1	0	1	L13, R13
1	1	1	0	Mute
1	1	1	1	Mute

L3, R3 Line select

b13	b12	b11	b10	L3, R3OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
1	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	L12, R12
1	1	0	1	L13, R13
1	1	1	0	Mute
1	1	1	1	Mute

L4, R4 Line select

b17	b16	b15	b14	L4, R4OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
1	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	L12, R12
1	1	0	1	L13, R13
1	1	1	0	Mute
1	1	1	1	Mute

OUT1 select

b21	b20	L1, R1OUT
0	0	Stereo
0	1	Mono1
1	0	Mono2
1	1	Don't Use

OUT2 select

b23	b22	L2, R2OUT
0	0	Stereo
0	1	Mono1
1	0	Mono2
1	1	Don't Use

OUT3 select

b21	b20	L1, R1OUT
0	0	Stereo
0	1	Mono1
1	0	Mono2
1	1	Don't Use

Mono1: L→L, R OUT

Mono2: R→L, R OUT

OUT4 select

b27	b26	L4, R4OUT
0	0	Stereo
0	1	Mono1
1	0	Mono2
1	1	Don't Use

OUT1 Gain Switch

b34	Gain
0	0dB
1	12dB

Out1 PowerSave select

b30	L1, R1OUT
0	Active
1	PowerSave

Out2 PowerSave select

b31	L2, R2OUT
0	Active
1	PowerSave

Out3 PowerSave select

b32	L3, R3OUT
0	Active
1	PowerSave

Out4 PowerSave select

b33	L4, R4OUT
0	Active
1	PowerSave

[Status registers]

MM1699 does not provide device information return processing to the master. When R/W bit is set to 1, all the status registers return 1. Then, any switch control is not performed.

S	Slave address							R/W	A	DATA1								A	P
	1	0	0	1	0	0	1	0		1	1	1	1	1	1	1	1		
	Address byte									Status byte									

*SA: Slave Acknowledge

*NA: Non Acknowledge

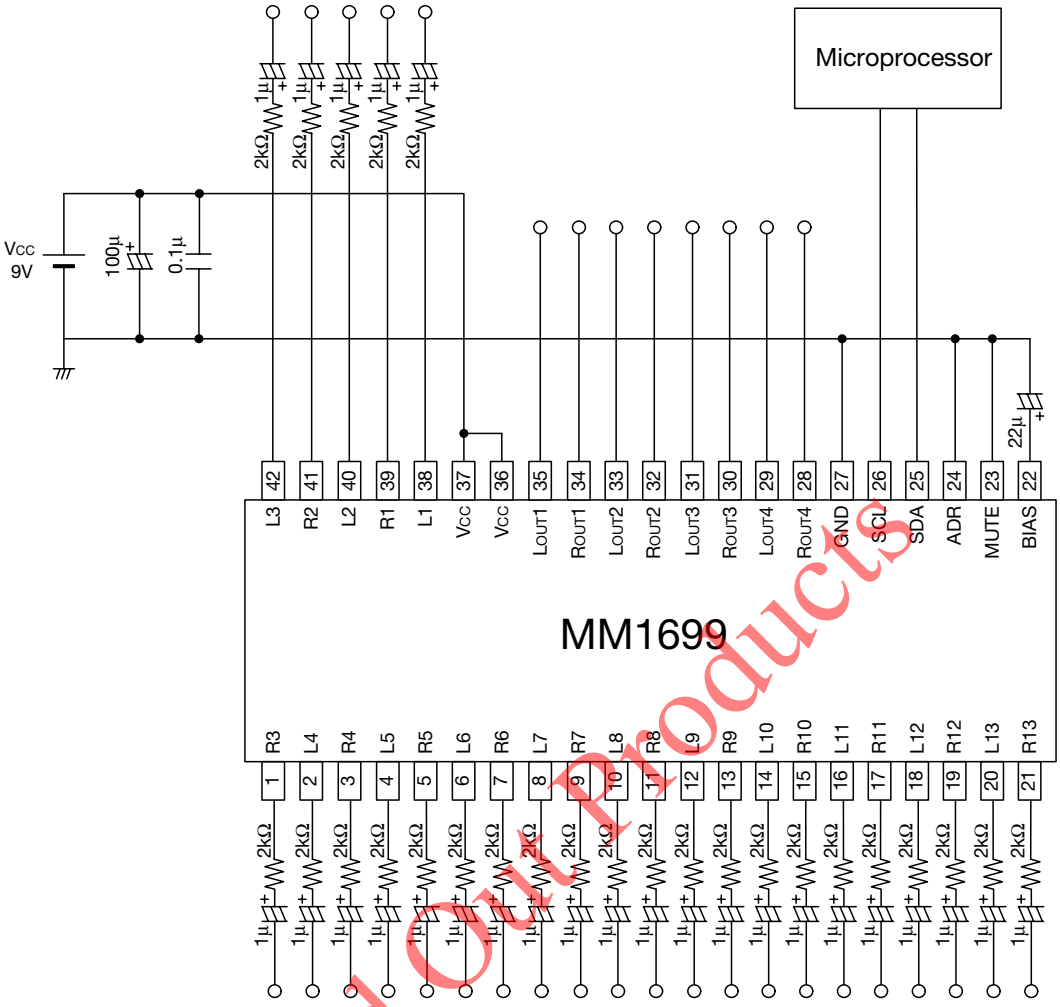
· Operation of Mute pin

When Mute pin is set to "H", all the audio output pins are connected to internal bias voltage. When Mute level returns from "H" to "L", audio output select returns to the previous condition.

Mute select

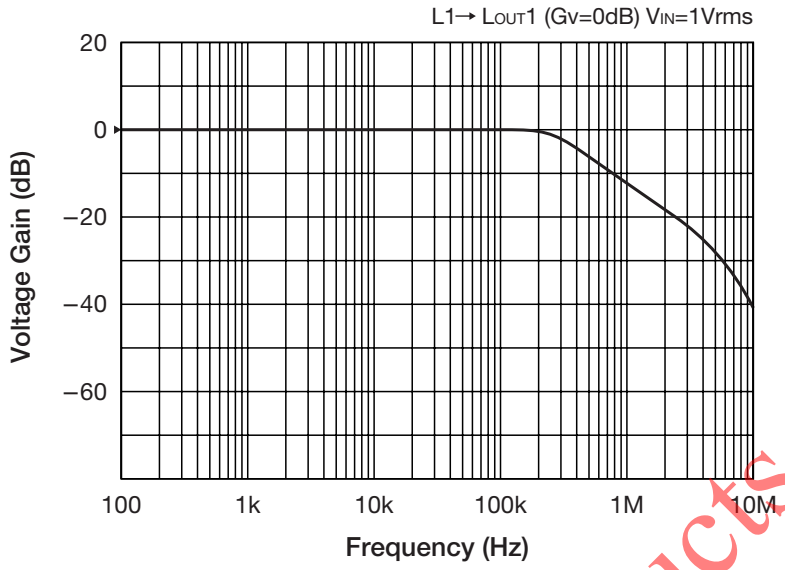
Mute	Output
H	Mute
L	Active

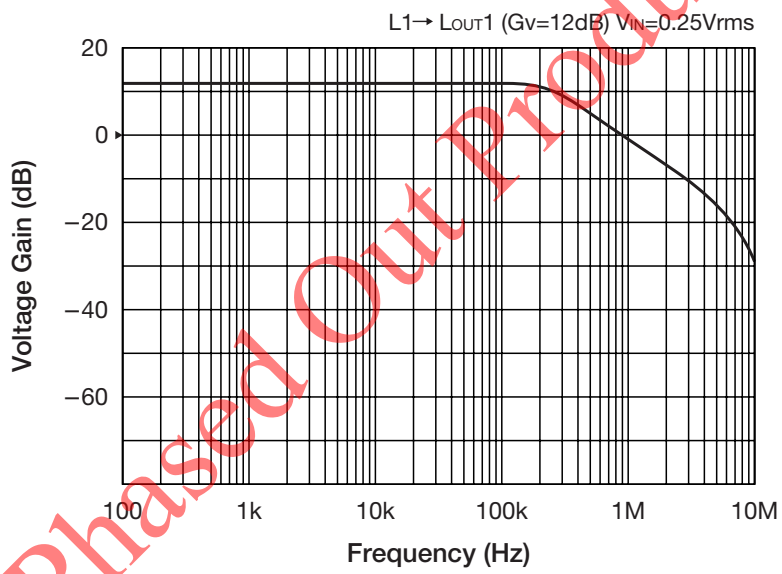
Application Circuit



Characteristics

Frequency characteristic





Total harmonic distortion - input voltage