

I²C Bus Control Video Switch IC

Monolithic IC MM1793XQ

Outline

With the start of the digital terrestrial broadcasting, we feel the pictures of high-definition quality familiar to ourselves. Together with the advent of the digital terrestrial broadcasting, the FPD is becoming more popular and its price has become reasonable for the consumers. FPD-TVs have beefed up with the additional functions to allow the connection of a variety of external equipment. Against these backgrounds, solutions to implement multiple inputs and multiple functions in one chip have to be developed for the video switches that input the image of high-definition quality.

This IC can support the video signal format of 1080p that is required to input the signal of high-definition image quality. In addition, it has the multiple-function circuit that are composed of 8-bit VCA, LPF switching and FLAG circuits, and this circuit can implement simple development design and the savings in the space for packaging footprint.

Features

1. Integrates the 8-bit VCA circuit that can tune variations between tuners.
2. Integrates the function to monitor the connection of the external input (FLAG function) to lower the load of the microcomputer.
3. Selectable one of three LPF cutoff frequencies so that the selected frequency can be compatible with the resolution and sampling frequency.
($f_c=6.75\text{MHz}$, 13.5MHz , or 37.5MHz)

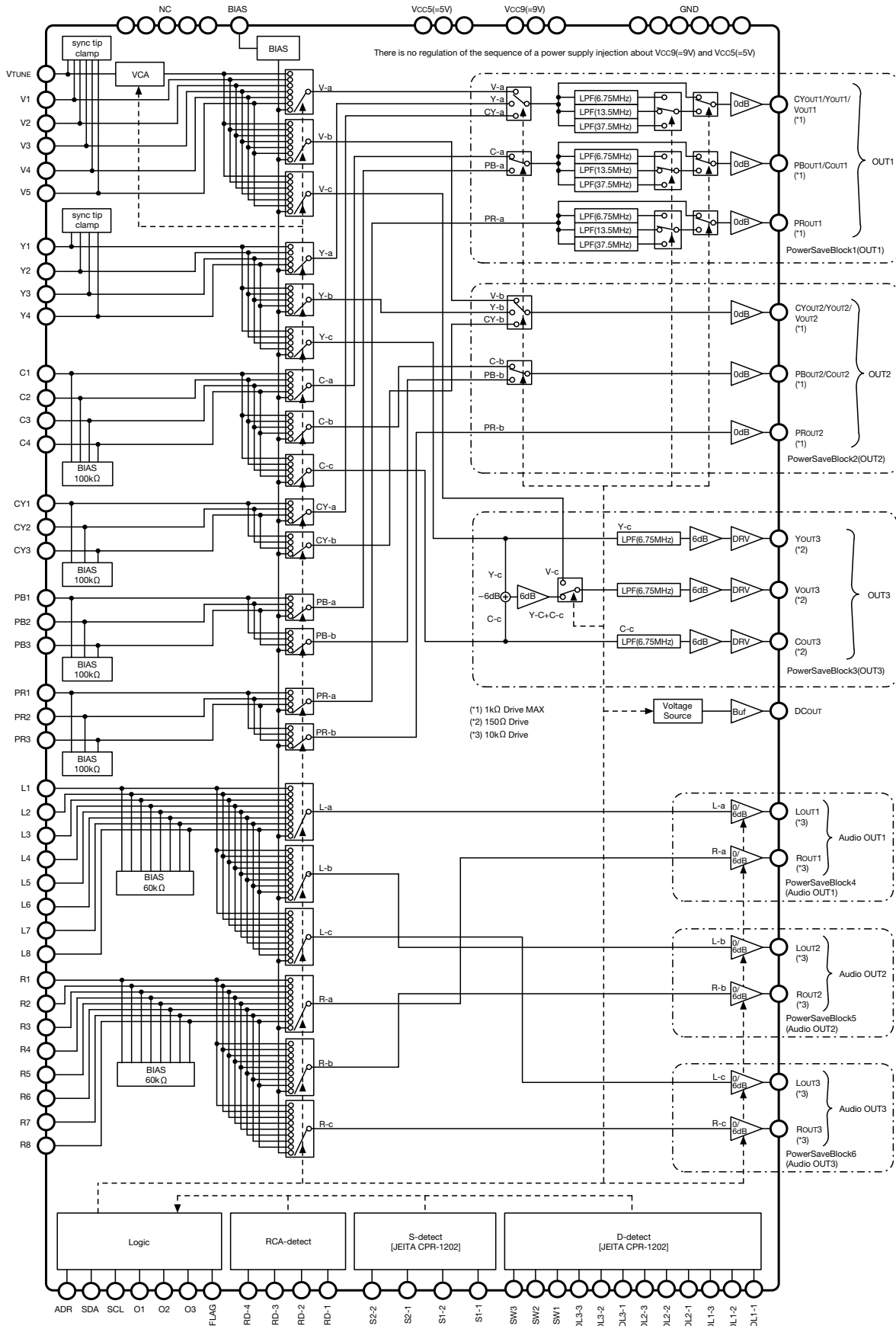
Packages

QFP-100

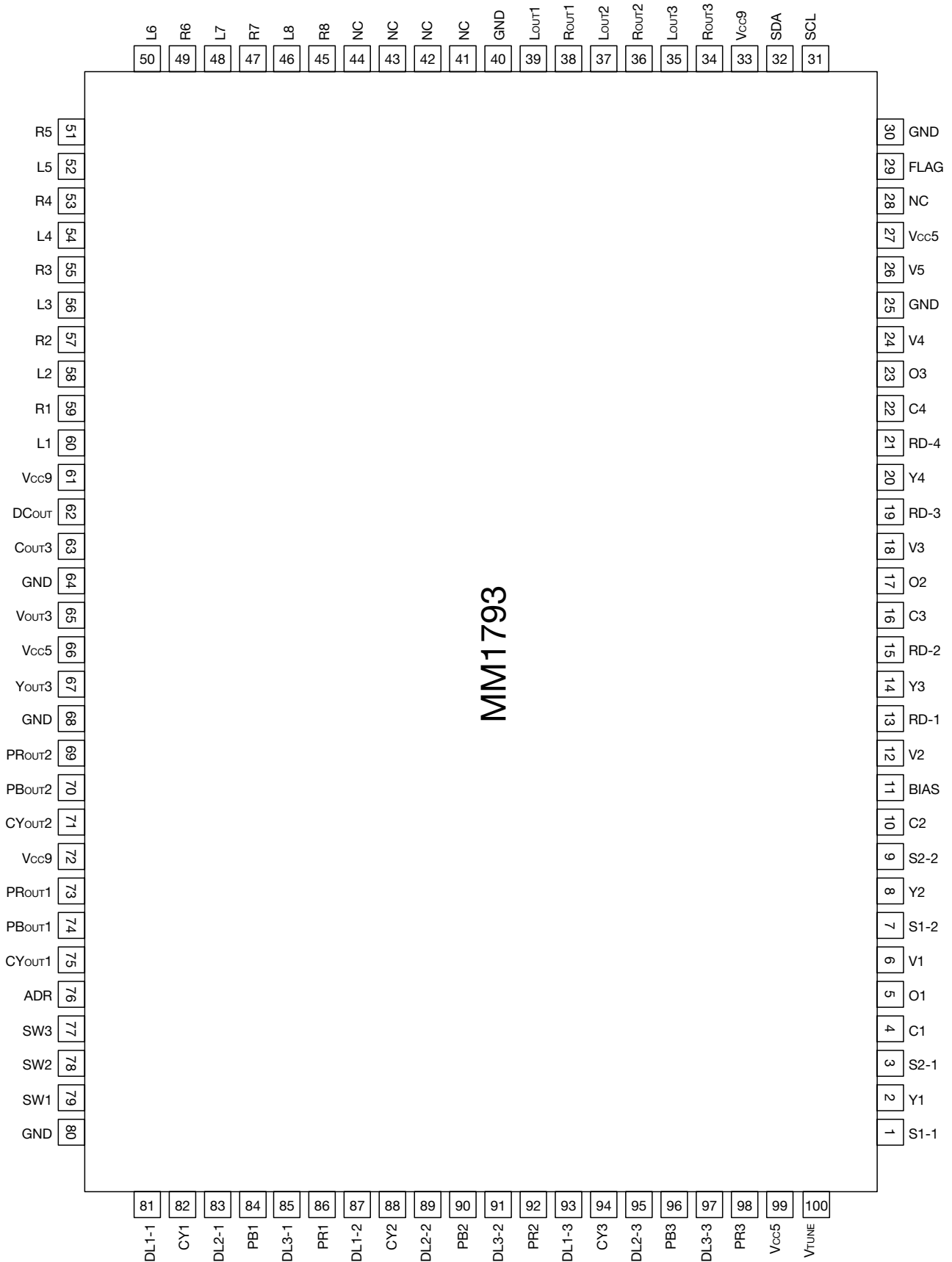
Applications

1. LCD-TV
 2. PDP-TV
-

Block Diagram

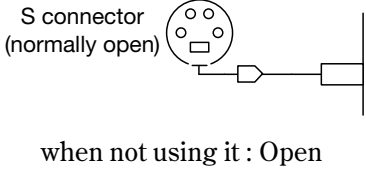
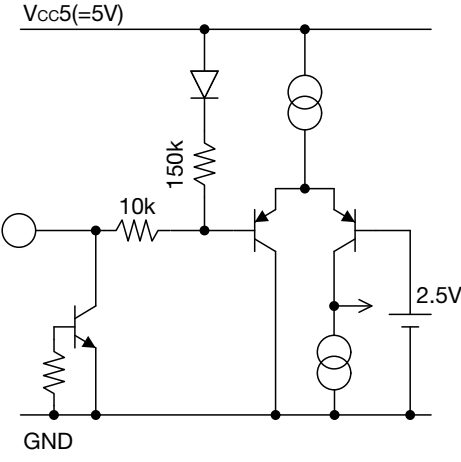
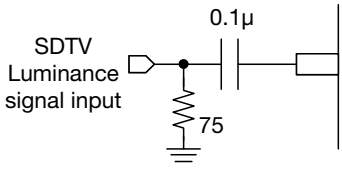
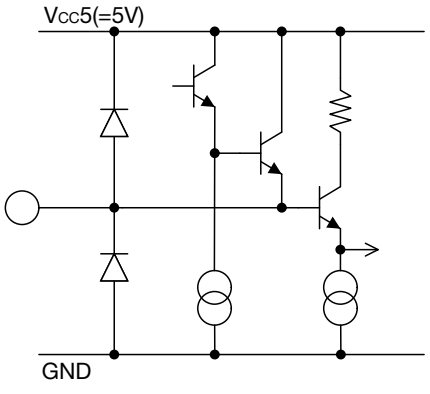
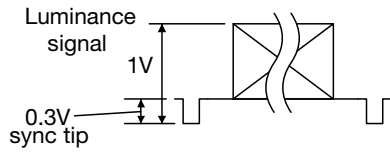


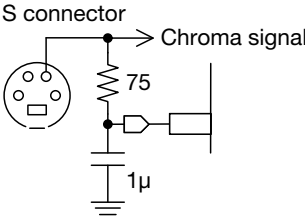
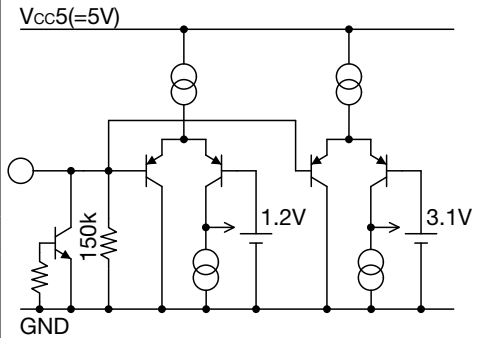
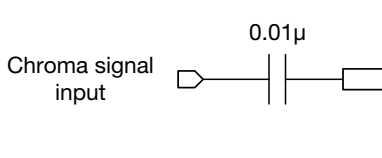
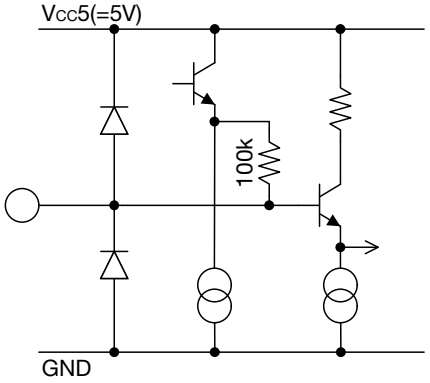
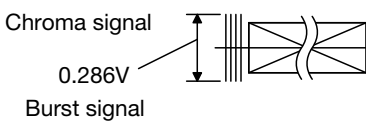
Pin Assignment

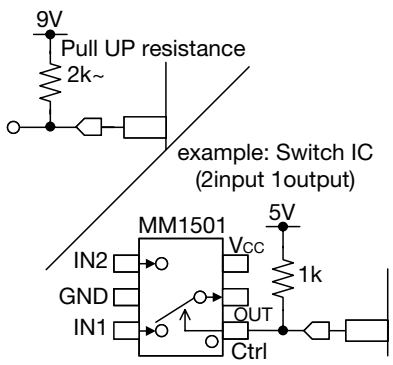
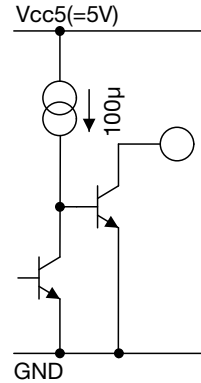
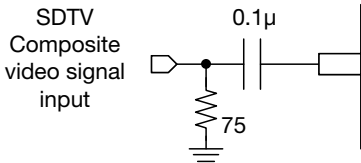
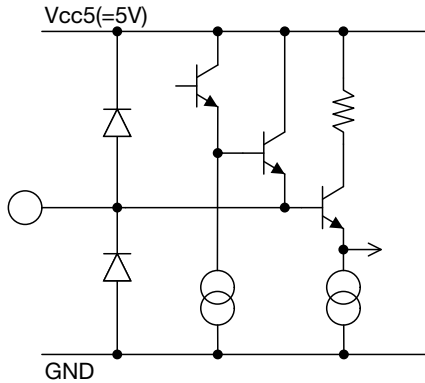
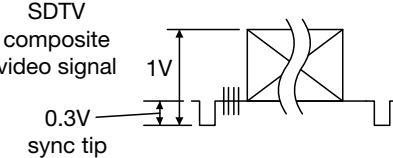


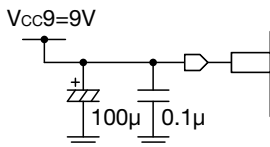
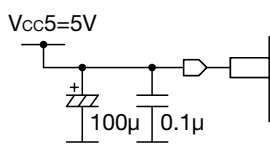
1	S1-1	21	RD-4	41	NC	61	Vcc9	81	DL1-1
2	Y1	22	C4	42	NC	62	DCour	82	CY1
3	S2-1	23	O3	43	NC	63	Cout3	83	DL2-1
4	C1	24	V4	44	NC	64	GND	84	PB1
5	O1	25	GND	45	R8	65	Vout3	85	DL3-1
6	V1	26	V5	46	L8	66	Vcc5	86	PR1
7	S1-2	27	Vcc5	47	R7	67	Yout3	87	DL1-2
8	Y2	28	NC	48	L7	68	GND	88	CY2
9	S2-2	29	FLAG	49	R6	69	PRout2	89	DL2-2
10	C2	30	GND	50	L6	70	PBout2	90	PB2
11	BIAS	31	SCL	51	R5	71	CYout2	91	DL3-2
12	V2	32	SDA	52	L5	72	Vcc9	92	PR2
13	RD-1	33	Vcc9	53	R4	73	PRout1	93	DL1-3
14	Y3	34	Rout3	54	L4	74	PBout1	94	CY3
15	RD-2	35	Lout3	55	R3	75	CYout1	95	DL2-3
16	C3	36	Rout2	56	L3	76	ADR	96	PB3
17	O2	37	Lout2	57	R2	77	SW3	97	DL3-3
18	V3	38	Rout1	58	L2	78	SW2	98	PR3
19	RD-3	39	Lout1	59	R1	79	SW1	99	Vcc5
20	Y4	40	GND	60	L1	80	GND	100	VTUNE

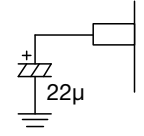
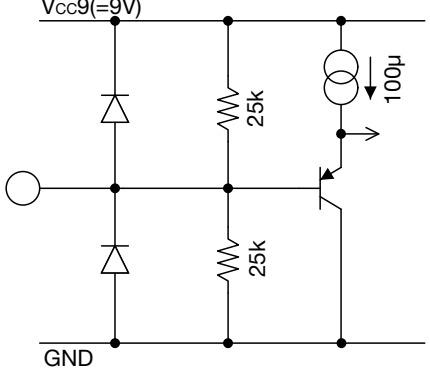
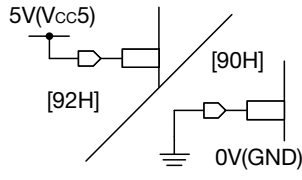
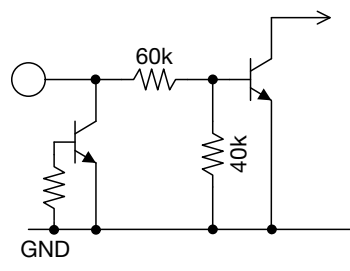
Pin Description

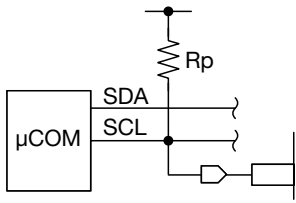
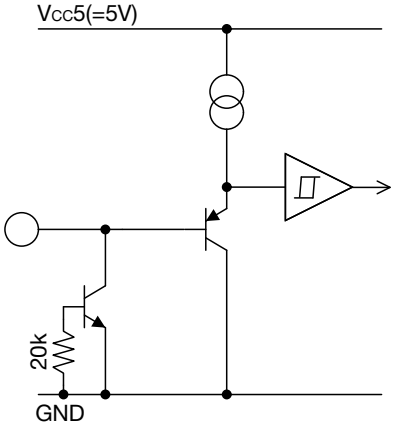

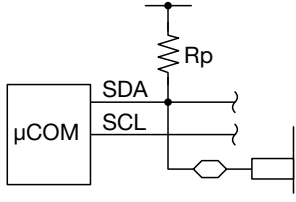
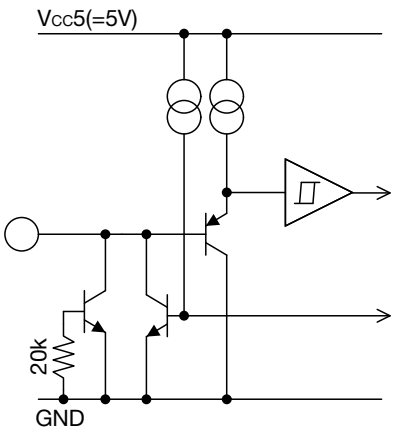
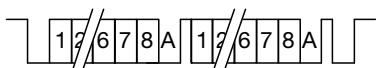
Pin No.	Pin name	Pin description	
1 7	S1-1 S1-2	Function	
		The terminal which detects the connection state of S connector A detected result is reflected in a status register. (refer to p.48~p.50) threshold : 2.4V typ. Input Impedance : 160kΩ typ.	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
Input signal			
		DC voltage : 0V(GND) or OPEN Note : When you impress voltage to a terminal, make it less than [6V].	
2 8 14 20	Y1 Y2 Y3 Y4	Function	
		Luminance signal input Input Clamp. Pin Voltage : 2.2V typ. Input Dynamic Range : 1.3 Vp-p min.	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
Input signal			
		 <p>Luminance signal 1V 0.3V sync tip</p>	

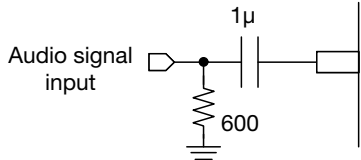
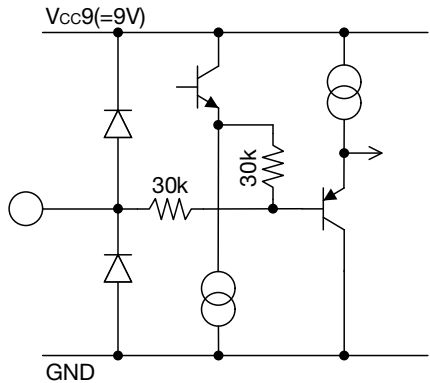
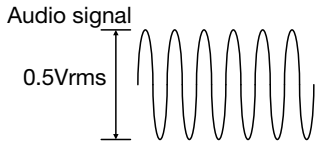
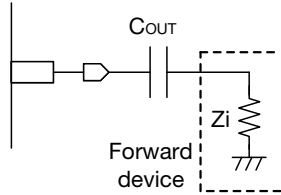
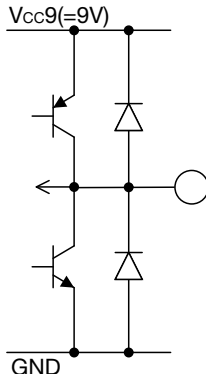
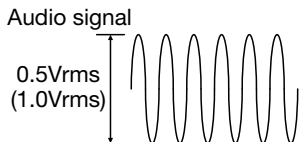
Pin No.	Pin name	Pin description									
3 9	S2-1 S2-2	Function									
		<p>The terminal which detects the aspect ratio information of S connector. A detected result is reflected in a status register. (refer to p.48-p.50)</p> <p>threshold1 : 1.2V typ. threshold2 : 3.1V typ. Input Impedance : 150kΩ typ.</p>									
		External circuit									
		Equivalent circuit diagram									
		 <p>when not using it : Open</p>									
		Input signal									
		<p>DC voltage :</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>S2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </tbody> </table>		S2	L	0V	M	1.4-2.4V	H	3.5-5V	
	S2										
L	0V										
M	1.4-2.4V										
H	3.5-5V										
4 10 16 22	C1 C2 C3 C4	Function									
		<p>Chroma signal input</p> <p>Input Bias Pin Voltage : 2.9V typ. Input Impedance : 100kΩ typ. Input Dynamic Range : 1.3 Vp-p min.</p>									
		External circuit									
		Equivalent circuit diagram									
		 <p>when not using it : Open</p>									
		Input signal									
											

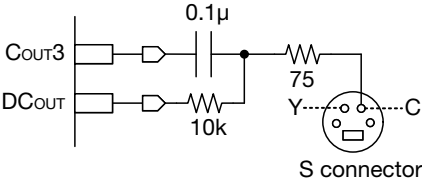
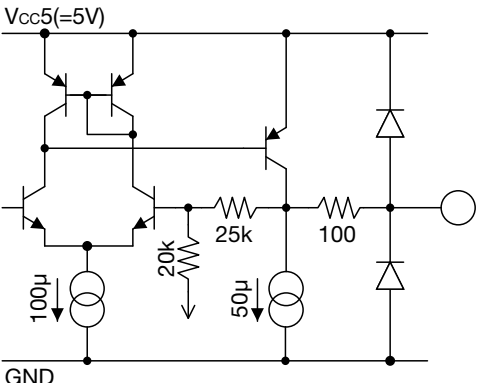
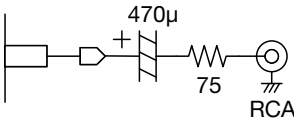
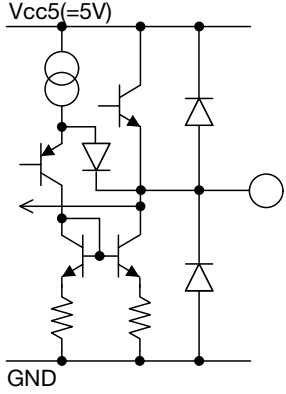
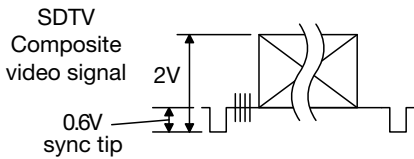
Pin No.	Pin name	Pin description																		
5 17 23	O1 O2 O3	Function																		
		<p>Output Port It is the open collector type general-purpose output port in which I²C control is possible.</p> <p>Sink Current : 5mA min.</p>																		
		External circuit	Equivalent circuit diagram																	
		 <p>when not using it : Open</p>																		
		Output signal																		
		<p>DC voltage :</p> <table border="1" style="display: inline-table; margin-right: 20px;"> <tr><td>b53</td><td>O1(5pin)</td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open(High)</td></tr> </table> <table border="1" style="display: inline-table; margin-right: 20px;"> <tr><td>b52</td><td>O2(17pin)</td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open(High)</td></tr> </table> <table border="1"> <tr><td>b51</td><td>O3(23pin)</td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open(High)</td></tr> </table>	b53	O1(5pin)	0	Low	1	Open(High)	b52	O2(17pin)	0	Low	1	Open(High)	b51	O3(23pin)	0	Low	1	Open(High)
b53	O1(5pin)																			
0	Low																			
1	Open(High)																			
b52	O2(17pin)																			
0	Low																			
1	Open(High)																			
b51	O3(23pin)																			
0	Low																			
1	Open(High)																			
6 12 18 24 26 100	V1 V2 V3 V4 V5 V _{TUNE}	Function																		
		<p>Composite signal input Built-in VCA circuit (V_{TUNE} Input). (refer to p.44) Maximum Voltage gain : 1.75V typ. Minimum Voltage gain : 0.5V typ. Level Control sensitivity : 4.9mV/bit typ.(at 1V_{p-p} Input)</p> <p>Input Clamp Pin Voltage : 2.2V typ. Input Dynamic Range : 1.3 V_{p-p} min.</p>																		
		External circuit	Equivalent circuit diagram																	
		 <p>when not using it : Open</p>																		
		Input signal																		
																				

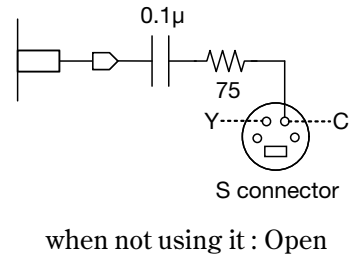
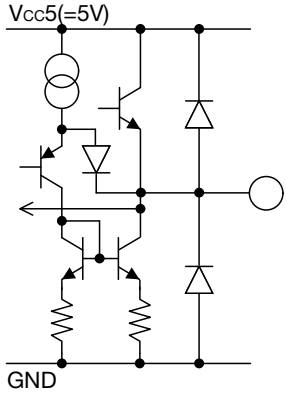
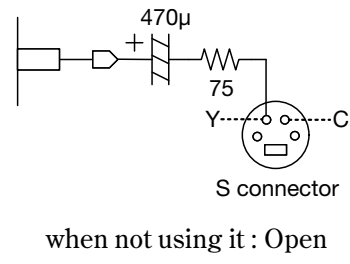
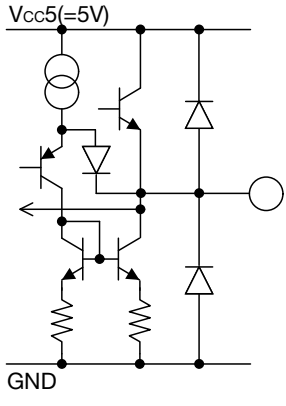
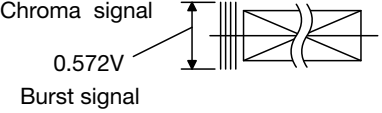
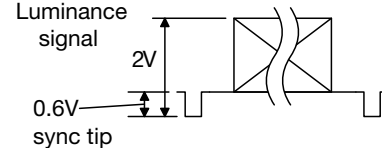
Pin No.	Pin name	Pin description	
33 61 72	Vcc9	Function	
		<p>Voltage Supply 1</p> <p>It is a supply voltage impression terminal. Please impress 9V. 33 pin, 61 pin and 72 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about Vcc9 (9V) and Vcc5 (5V).</p> <p>Note : Please arrange a bypass capacitor to the terminal latest as much as possible.</p>	
		External circuit	Equivalent circuit diagram
			
		Input signal	
		DC voltage : +8.0V~+10.0V	
27 66 99	Vcc5	Function	
		<p>Voltage Supply 2</p> <p>It is a supply voltage impression terminal. Please impress 5V. 27 pin, 66pin and 99 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about Vcc9 (9V) and Vcc5 (5V).</p> <p>Note : Please arrange a bypass capacitor to the terminal latest as much as possible.</p>	
		External circuit	Equivalent circuit diagram
			
		Input signal	
		DC voltage : +4.5V~+5.5V	
25 30 40 64 68 80	GND	Function	
		<p>GND</p> <p>It is a GND terminal. 25pin, 30pin, 40pin, 64pin, 68pin and 80pin short-circuit inside IC.</p>	
		External circuit	Equivalent circuit diagram
		<p style="text-align: center;">—</p>	
		Input signal	
		<p style="text-align: center;">—</p>	

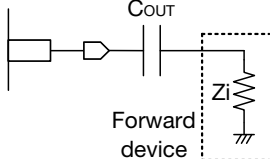
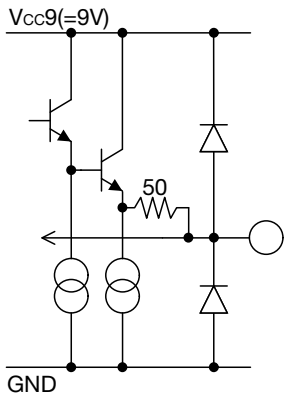
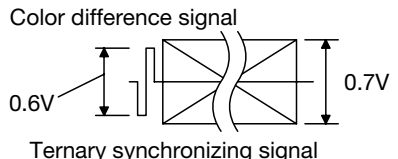
Pin No.	Pin name	Pin description	
11	BIAS	Function	
		<p>BIAS</p> <p>All the criteria voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor for criteria voltage stabilization.</p> <p>Input Impedance : 12.6kΩ typ.</p>	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
Input signal			
		Function	
76	ADR	<p>Slave Address select pin</p> <p>The I²C slave addresses 90H and 92H can be chosen with the voltage impressed to this terminal. It is set to 90H by Low, and is set to 92H by High.</p> <p>threshold : 1.75V typ.</p> <p>Input Impedance : 100kΩ typ.</p>	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
		Input signal	
		DC voltage : 0V(GND) or 5V(Vcc5)	

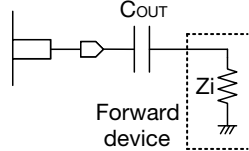
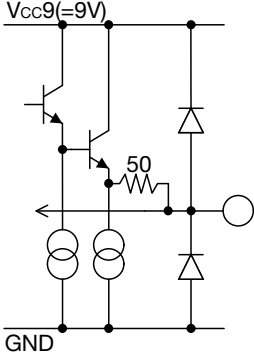
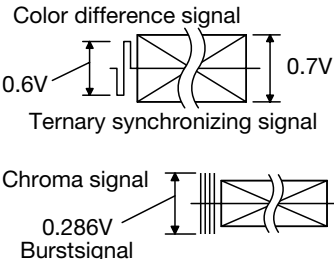
Pin No.	Pin name	Pin description
31	SCL	Function
		<p>Clock input of I²C bus It is the terminal which connects the SCL line of I²Cbus.</p>
		External circuit
		Input signal
		Equivalent circuit diagram
		
<p>Input signal Clock signal</p> 		
32	SDA	Function
		<p>DATA I/O of I²C bus It is the terminal which connects the SDA line of I²Cbus.</p>
		External circuit
		Input signal
		Equivalent circuit diagram
		
<p>Input signal Control registers Output signal States registers</p> 		

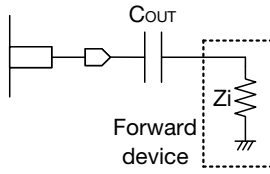
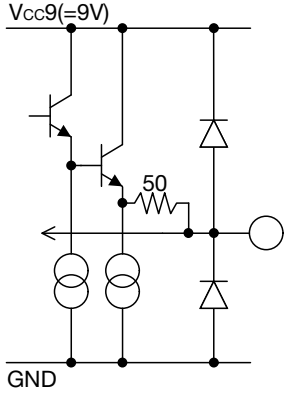
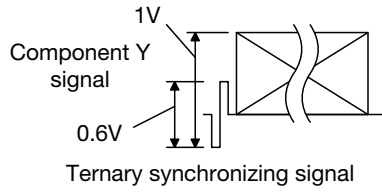
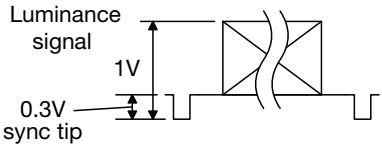
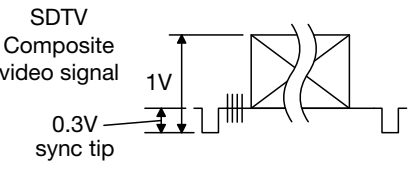
Pin No.	Pin name	Pin description	
45~60	L1~L8 R1~R8	Function	
		<p>Audio line input</p> <p>Pin to input audio signals. It includes 8 channels; L1-L8, R1-R8.</p> <p>Terminal voltage : 3.80V typ. Input Impedance : 60kΩ typ. Input dynamic range : 3Vrms typ.</p>	
		External circuit	
		Equivalent circuit diagram	
		 <p>when not using it : connect to GND or Vcc9</p>	
		Input signal	
			
34~39	LOUT1~3 ROUT1~3	Function	
		<p>Audio line output</p> <p>Pin to output audio signals</p> <p>Voltage gain of 0dB/6dB is controllable by a control registers (b44-b46). Audio line Output1 (b46=0 : 0dB mode, b46=1 : 6dB mode) Audio line Output2 (b45=0 : 0dB mode, b45=1 : 6dB mode) Audio line Output3 (b44=0 : 0dB mode, b44=1 : 6dB mode)</p> <p>Terminal voltage : 4.50V typ. Voltage gain : 0dB/6dB typ. Frequency characteristic : -3dB at 50kHz min.</p>	
		External circuit	
		Equivalent circuit diagram	
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p>*f_{CL}=1~10Hz</p> <p>when not using it : Open</p>	
		Output signal	
			

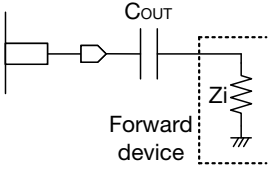
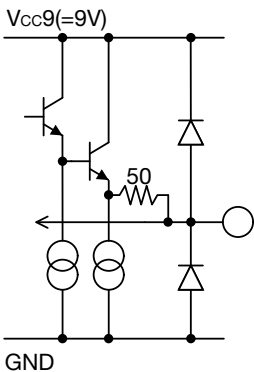
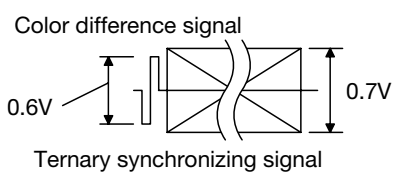
Pin No.	Pin name	Pin description																					
62	DCOUT	Function																					
		<p>DC output for S terminal It is the terminal which outputs S1/S2 signal of S terminal. The ternary output of L/M/H is controllable by I2C control. (refer to p.44)</p>																					
		External circuit																					
		Equivalent circuit diagram																					
		 <p>when not using it : Open</p>																					
		Output signal																					
		<p>DC voltage :</p> <table border="1" data-bbox="523 884 944 1070"> <thead> <tr> <th></th> <th>b27</th> <th>b26</th> <th>DCOUT</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0</td> <td>0</td> <td>0V</td> </tr> <tr> <td>M</td> <td>0</td> <td>1</td> <td>2.2V</td> </tr> <tr> <td>H</td> <td>1</td> <td>0</td> <td>5V</td> </tr> <tr> <td>-</td> <td>1</td> <td>1</td> <td>Hi-Imp</td> </tr> </tbody> </table>		b27	b26	DCOUT	L	0	0	0V	M	0	1	2.2V	H	1	0	5V	-	1	1	Hi-Imp	
	b27	b26	DCOUT																				
L	0	0	0V																				
M	0	1	2.2V																				
H	1	0	5V																				
-	1	1	Hi-Imp																				
65	VOUT3	Function																					
		<p>monitor output(composite signal) It is a terminal for a composite signal external output. V or Y+C (MIX) can be chosen. (refer to p.44)</p> <p>Pin Voltage : 1.2V typ. Load Resistance : 150Ω Stray Capacitance : 20pF max.</p>																					
		External circuit																					
		Equivalent circuit diagram																					
		 <p>when not using it : Open</p>																					
		Output signal																					
																							

Pin No.	Pin name	Pin description	
63	COUT3	Function	
		<p>monitor output (chroma signal) It is a terminal for the chroma signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 150Ω Stray Capacitance : 20pF max.</p>	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
67	YOUT3	Function	
		<p>monitor output (Luminance signal) It is a terminal for a Luminance signal external output.</p> <p>Pin Voltage : 1.2V typ. Load Resistance : 150Ω Stray Capacitance : 20pF max.</p>	
		External circuit	Equivalent circuit diagram
		 <p>when not using it : Open</p>	
Output signal		 <p>Chroma signal 0.572V Burst signal</p>  <p>Luminance signal 2V 0.6V sync tip</p>	

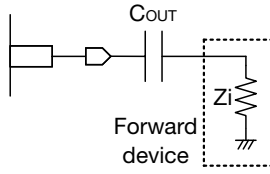
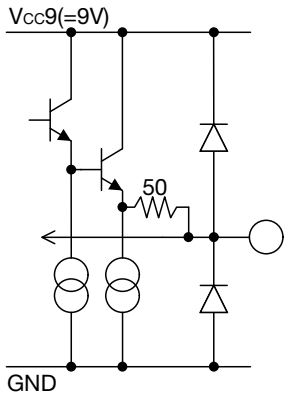
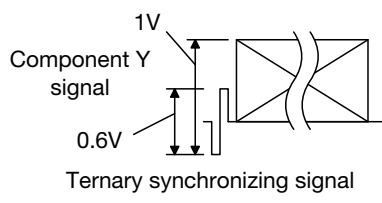
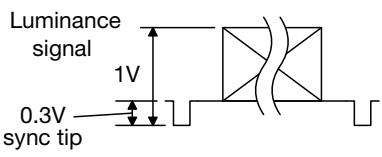
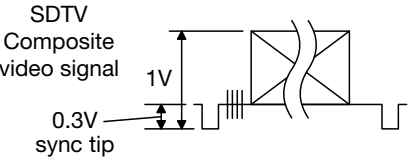
Pin No.	Pin name	Pin description	
69	PROUT2	Function	
		<p>Color difference signal output It is a terminal for a Color difference signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f_{CL}=1~10Hz</p> <p style="text-align: center;">when not using it : Open</p>	
		Output signal	
 <p>Color difference signal</p> <p>0.6V</p> <p>Ternary synchronizing signal</p> <p>0.7V</p>			

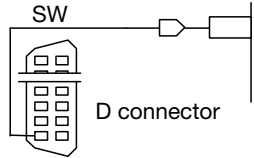
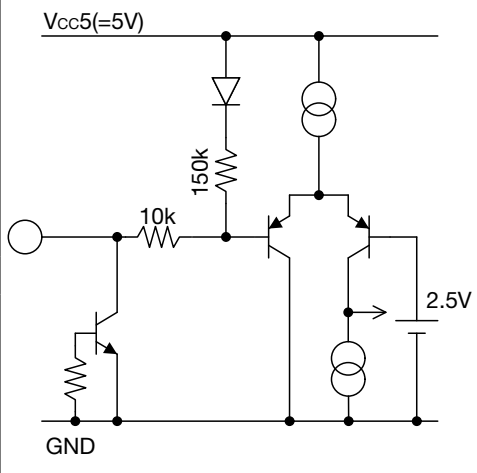
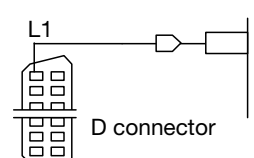
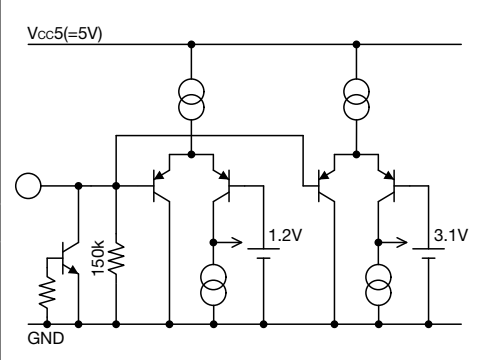
Pin No.	Pin name	Pin description	
70	PBOUT2 /COUT2	Function	
		<p>Color difference signal or Chroma signal output It is a terminal for a Color difference or Chroma signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f_{CL}=1~10Hz</p> <p>when not using it : Open</p>	
		Output signal	
 <p>Color difference signal 0.6V to 0.7V Ternary synchronizing signal</p> <p>Chroma signal 0.286V Bursts</p>			

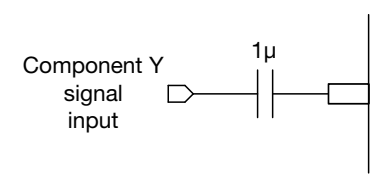
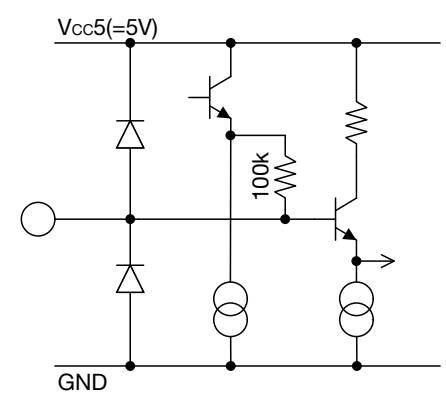
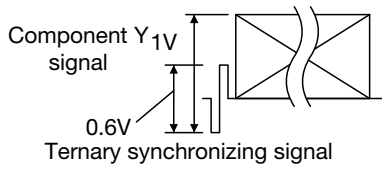
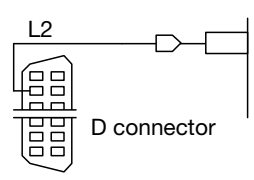
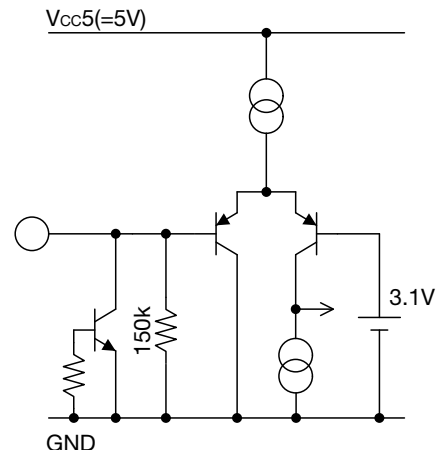
Pin No.	Pin name	Pin description	
71	CYOUT2 /YOUT2 /VOUT2	Function	
		<p>Color difference signal, Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		<div style="display: flex; justify-content: space-between;"> <div data-bbox="582 577 853 750">  </div> <div data-bbox="1077 952 1364 1344">  </div> </div> $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f_{CL}=1~10Hz</p> <p style="text-align: center;">when not using it : Open</p>	
		Output signal	
<div style="display: flex; flex-direction: column; gap: 10px;"> <div data-bbox="534 1064 917 1254">  <p>Ternary synchronizing signal</p> </div> <div data-bbox="566 1332 949 1478">  <p>Luminance signal</p> </div> <div data-bbox="534 1568 949 1736">  <p>SDTV Composite video signal</p> </div> </div>			

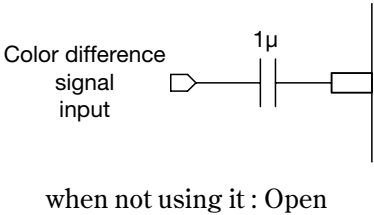
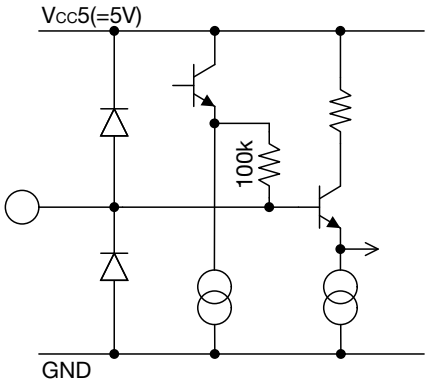
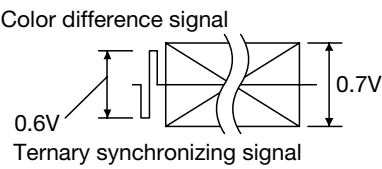
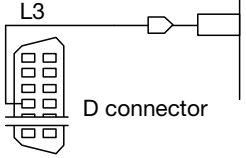
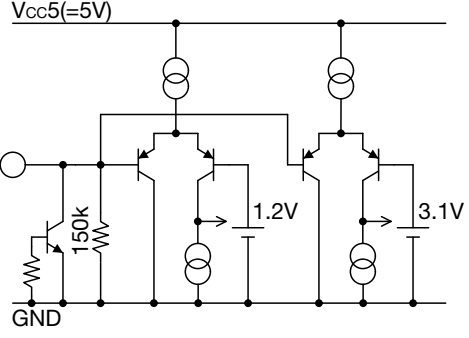
Pin No.	Pin name	Pin description	
73	PROUT1	Function	
		<p>Color difference signal output It is a terminal for a Color difference signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f_{CL}=1~10Hz</p> <p style="text-align: center;">when not using it : Open</p>	
		Output signal	
 <p style="text-align: center;">Color difference signal 0.6V</p> <p style="text-align: center;">Ternary synchronizing signal 0.7V</p>			

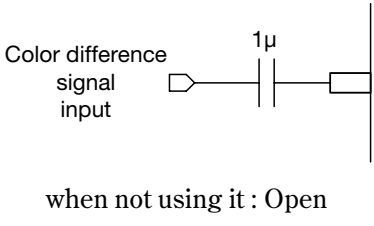
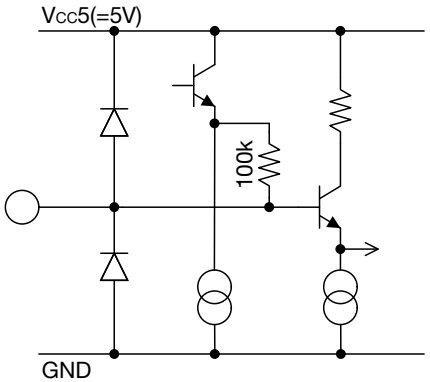
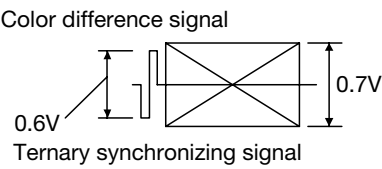
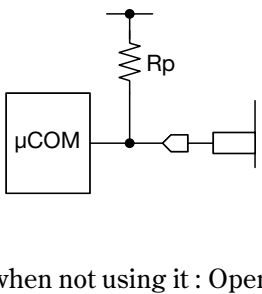
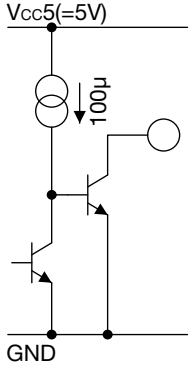
Pin No.	Pin name	Pin description	
74	PBOUT1 /COUT1	Function	
		<p>Color difference signal or Chroma signal output It is a terminal for a Color difference or Chroma signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		<div style="display: flex; justify-content: space-around;"> <div data-bbox="587 539 858 703"> </div> <div data-bbox="1091 734 1347 1099"> </div> </div>	
		when not using it : Open	
Output signal			
<div style="display: flex; flex-direction: column; gap: 10px;"> <div data-bbox="544 969 924 1128"> <p>Color difference signal</p> <p>Ternary synchronizing signal</p> </div> <div data-bbox="539 1218 924 1330"> <p>Chroma signal</p> <p>0.286V Burst signal</p> </div> </div>			

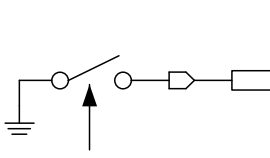
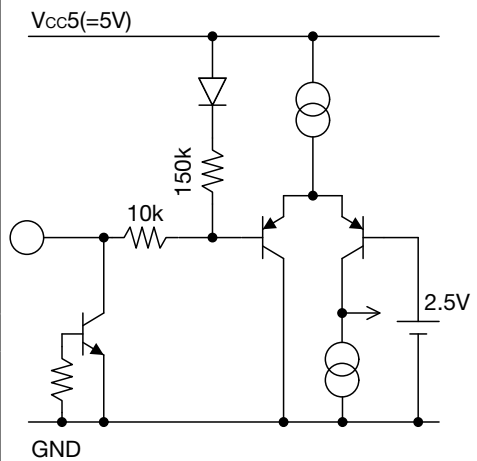
Pin No.	Pin name	Pin description	
75	CYOUT1 /YOUT1 /VOUT1	Function	
		<p>Color difference signal , Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output.</p> <p>Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capacitance : 10pF max.</p>	
		External circuit	Equivalent circuit diagram
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f_{CL}=1~10Hz</p>	
		when not using it : Open	
Output signal			
<p>Component Y signal</p>  <p>Ternary synchronizing signal</p>			
<p>Luminance signal</p>  <p>0.3V sync tip</p>			
<p>SDTV Composite video signal</p>  <p>0.3V sync tip</p>			

Pin No.	Pin name	Pin description					
77 78 79	SW3 SW2 SW1	Function					
		The terminal which detects the connection state of D connector. A detected result is reflected in a status register. (refer to p.48-p.50) threshold : 2.4V typ. Input Impedance : 160kΩ typ.					
		External circuit	Equivalent circuit diagram				
		 <p>when not using it : Open</p>					
		Input signal					
DC voltage : 0V (GND) or OPEN Note : When you impress voltage to a terminal, make it less than [6V].							
81 87 93	DL1-1 DL1-2 DL1-3	Function					
		The terminal which detects the number-of-scanning-lines information on D connector. A detected result is reflected in a status register. (refer to p.48-50) threshold1 : 1.2V typ. threshold2 : 3.1V typ. Input Impedance : 150kΩ typ.					
		External circuit	Equivalent circuit diagram				
		 <p>when not using it : Open</p>					
		Input signal					
DC voltage : <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </table>		L	0V	M	1.4-2.4V	H	3.5-5V
L	0V						
M	1.4-2.4V						
H	3.5-5V						

Pin No.	Pin name	Pin description							
82 88 94	CY1 CY2 CY3	Function							
		<p>Component Y signal input A RGB signal can also be inputted besides a component Y signal.</p> <p>Input Bias Pin Voltage : 2.9V typ. Input Impedance : 100kΩ typ. Input Dynamic Range : 1.6 Vp-p min.</p>							
		External circuit							
		Equivalent circuit diagram							
		 <p>Component Y signal input</p> <p>when not using it : Open</p>	 <p>Vcc5(=5V)</p> <p>GND</p>						
		Input signal							
		 <p>Component Y 1V signal</p> <p>0.6V Ternary synchronizing signal</p>							
83 89 95	DL2-1 DL2-2 DL2-3	Function							
		<p>The terminal which detects the I/P information of D connector. A detected result is reflected in a status register. (refer to p.48-p.50)</p> <p>threshold : 3.1V typ. Input Impedance : 150kΩ typ.</p>							
		External circuit							
		Equivalent circuit diagram							
		 <p>L2</p> <p>D connector</p> <p>when not using it : Open</p>	 <p>Vcc5(=5V)</p> <p>GND</p> <p>3.1V</p>						
		Input signal							
		<p>DC voltage :</p> <table border="1" data-bbox="542 1747 845 1859"> <tr> <td></td> <td>L2</td> </tr> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </table>		L2	L	0V	H	3.5-5V	
	L2								
L	0V								
H	3.5-5V								

Pin No.	Pin name	Pin description									
84 90 96	PB1 PB2 PB3	Function									
		<p>Color difference signal input A RGB signal can also be inputted besides a color-difference signal.</p> <p>Input Bias Pin Voltage : 2.9V typ. Pin Voltage : 100kΩ typ. Input Impedance : 1.6 Vp-p typ.</p>									
		External circuit									
		Equivalent circuit diagram									
											
		Input signal									
											
85 91 97	DL3-1 DL3-2 DL3-3	Function									
		<p>The terminal which detects the aspect ratio information of D connector. A detected result is reflected in a status register. (refer to p.48-p.50)</p> <p>threshold1 : 1.2V typ. threshold2 : 3.1V typ. Input Impedance : 150kΩ typ.</p>									
		External circuit									
		Equivalent circuit diagram									
											
		Input signal									
		<p>DC voltage :</p> <table border="1" data-bbox="542 1780 853 1937"> <tr> <td></td> <td>L3</td> </tr> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </table>		L3	L	0V	M	1.4-2.4V	H	3.5-5V	
	L3										
L	0V										
M	1.4-2.4V										
H	3.5-5V										

Pin No.	Pin name	Pin description						
86 92 98	PR1 PR2 PR3	Function						
		<p>Color difference signal input A RGB signal can also be inputted besides a color-difference signal.</p> <p>Input Bias Pin Voltage : 2.9V typ. Input Impedance : 100kΩ typ. Input Dynamic Range : 1.6 Vp-p typ.</p>						
		External circuit						
		Equivalent circuit diagram						
		Input signal						
		  <p>when not using it : Open</p>  <p>Color difference signal 0.6V Ternary synchronizing signal 0.7V</p>						
29	FLAG	Function						
		<p>The output terminal which monitor and detects a status register When status register information changes, an output is changed to Low. When status register information is readed, an output is changed to Open. It is the open collector type output port. (refer to p.50)</p> <p>Sink Current : 5mA min.</p>						
		External circuit						
		Equivalent circuit diagram						
		Output signal						
		 <p>when not using it : Open</p>  <p>DC voltage :</p> <table border="1" data-bbox="542 1870 1141 1993"> <tr> <td>Status register information</td> <td>FLAG(29pin)</td> </tr> <tr> <td>change</td> <td>Low</td> </tr> <tr> <td>readed</td> <td>Open(High)</td> </tr> </table>	Status register information	FLAG(29pin)	change	Low	readed	Open(High)
Status register information	FLAG(29pin)							
change	Low							
readed	Open(High)							

Pin No.	Pin name	Pin description			
13 15 19 21	RD-1 RD-2 RD-3 RD-4	Function			
		The terminal which detects the connection state of RCA connector A detected result is reflected in a status register. (refer to p.48-p.50) threshold : 2.4V typ. Input Impedance : 160kΩ typ.			
		External circuit	Equivalent circuit diagram		
		 <p>The signal which detects the connection state of RCA connector</p> <p>when not using it : Open</p>			
		Input signal			
		DC voltage : 0V (GND) or OPEN Note : When you impress voltage to a terminal, make it less than [6V].			
28 41 42 43 44	NC	Function			
		None Connection terminal			
		External circuit	Equivalent circuit diagram		
		—			
		Input signal		—	
		—			

Absolute Maximum Ratings (Except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-65~+150	°C
Operating temperature	T _{OPR}	-40~+85	°C
Supply voltage 1	V _{CC9MAX}	-0.2~+10.0	V
Supply voltage 2	V _{CC5MAX}	-0.2~+6.0	V
Input voltage 1	V _{IN1MAX}	-0.2~V _{CC9} +0.2	V
Input voltage 2	V _{IN2MAX}	-0.2~V _{CC5} +0.2	V
Output voltage 1	V _{OUT9MAX}	-0.2~V _{CC9} +0.2	V
Output voltage 2	V _{OUT5MAX}	-0.2~V _{CC5} +0.2	V
Output current	I _{OUTMAX}	25	mA
Junction temperature	T _{JMAX}	150	°C
Thermal resistance	θ _{j-c}	6.0	°C/W
Power dissipation (Note1)	P _d	3.6	W

Note1 : Board mounting power dissipation. Board size 193×189×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T _{OPR}	-40~+85	°C
Operating voltage 1	V _{CC9OP}	+8.0~+10.0	V
Operating voltage 2	V _{CC5OP}	+4.5~+5.5	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc9=9V, Vcc5=5V,VCA GAIN SELECT='66H')

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
Current consumption							
Current consumption	Vcc9 (9V)	ICC9-0	[I ² C BUS DATA= ' ALL 0 ']	36	60	84	mA
	Vcc5 (5V)	ICC5-0		60	100	140	
All Power save Current consumption							
Current consumption (at All PS mode)	Vcc9 (9V)	ICC9-0	[b05,b15,b25,b56,b55,b54 = ' 1,1,1,1,1 ']	5	10	15	mA
	Vcc5 (5V)	ICC5-0		30	50	70	
Block Current consumption							
Current consumption (at OUT1 block)	Vcc9 (9V)	ICC9-V1	Icc[b05 = ' 0 ']-Icc[b05 = ' 1 ']		30		mA
	Vcc5 (5V)	ICC5-V1			15		
Current consumption (at OUT2 block)	Vcc9 (9V)	ICC9-V2	Icc[b15 = ' 0 ']-Icc[b15 = ' 1 ']		15		mA
	Vcc5 (5V)	ICC5-V2			5		
Current consumption (at OUT3 block)	Vcc9 (9V)	ICC9-V3	Icc[b25 = ' 0 ']-Icc[b25 = ' 1 ']		0		mA
	Vcc5 (5V)	ICC5-V3			30		
Current consumption (at AUDIO OUT1 block)	Vcc9 (9V)	ICC9-A1	Icc[b56 = ' 0 ']-Icc[b56 = ' 1 ']		4		mA
Current consumption (at AUDIO OUT2 block)	Vcc9 (9V)	ICC9-A2	Icc[b55 = ' 0 ']-Icc[b55 = ' 1 ']		4		mA
Current consumption (at AUDIO OUT3 block)	Vcc9 (9V)	ICC9-A3	Icc[b54 = ' 0 ']-Icc[b54 = ' 1 ']		4		mA

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input pin voltage						
Input pin voltage 1 (V,Y)	V _{in1}	100,6,12,18,24,26,2,8,14,20 pin	1.7	2.2	2.7	V
Input pin voltage 2 (C,CY,PB,PR)	V _{in2}	4,10,16,22,82,84,86,88,90,92,94,96,98 pin	2.3	2.9	3.5	V
Input pin voltage 3 (L,R)	V _{in3}	45 ~ 60 pin	3.2	3.8	4.4	V
Output pin voltage (OUT1,2)						
Output pin voltage 1	V _{out1}	69,70,71,73,74,75 pin	2.0	2.4	2.8	V
Output pin voltage (OUT3)						
Output pin voltage 2 (V,Y)	V _{out2}	65,67 pin	0.8	1.2	1.6	V
Output pin voltage 3 (C)	V _{out3}	63 pin	2.0	2.4	2.8	V
Output pin voltage (Audio OUT1,2,3)						
Audio output pin voltage (L,R)	V _{out4}	34 ~ 39 pin	4.1	4.5	4.9	V
S-DCOUT pin output voltage						
S-DCOUT pin output voltage	L	V _{DCOUTL} 62 pin RL=10kΩ+100kΩ	GND	0.1	0.5	V
	M	V _{DCOUTM} 62 pin RL=10kΩ+100kΩ	1.6	2.1	2.4	V
	H	V _{DCOUTH} 62 pin RL=10kΩ+100kΩ	4.3	4.6	V _{cc5}	V
Bias input impedance						
CIN input impedance	Z _{CIN}	4,10,16,22 pin	70	100	130	kΩ
CYIN input impedance	Z _{CYIN}	82,88,94 pin	70	100	130	kΩ
PbIN input impedance	Z _{PbIN}	84,90,96 pin	70	100	130	kΩ
PrIN input impedance	Z _{PrIN}	86,92,98 pin	70	100	130	kΩ
LIN input impedance	Z _{LIN}	60,58,56,54,52,50,48,46 pin	47	60	73	kΩ
RIN input impedance	Z _{RIN}	59,57,55,53,51,49,47,45 pin	47	60	73	kΩ

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
V_{TUNE} (100pin) electrical characteristics							
VCA Maximum Voltage gain	G _{VVCAmax}	V _{out} (V _{TUNE} =V _{in1} +1V) -V _{out} (V _{TUNE} =V _{in1}) 71,75 pin [VCA GAIN SELECT='FFH']	1.40	1.75	2.10	V	
VCA Minimum Voltage gain	G _{VVCAmin}	V _{out} (V _{TUNE} =V _{in1} +1V) -V _{out} (V _{TUNE} =V _{in1}) 71,75 pin [VCA GAIN SELECT='00H']	0.40	0.50	0.60	V	
VCA Level Control sensitivity	S _{VCA}	SIN wave : 1V f=100kHz 71,75 pin	0	4.9	9.8	mV/bit	
VCA Level linearity error (Note2)	LE _{VCA}	SIN wave : 1V f=100kHz 71,75 pin	-1.5		1.5	LSB	
VOUT3 (65pin) electrical characteristics							
VOUT3 Voltage gain	G _{VVOUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB	
VOUT3 Frequency characteristic	with filter	f _{1VOUT3}	SIN wave : 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f _{2VOUT3}	SIN wave : 1V 27MHz/100kHz		-33.0	-24.0	dB
VOUT3 Input dynamic range	DR _{VOUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V	
VOUT3 Group delay	with filter	t _{GD VOUT3}	at 100kHz		55	ns	
VOUT3 Group delay deviation 1	with filter	Δt _{1GD VOUT3}	to 3.58MHz		4	20	ns
VOUT3 Group delay deviation 2	with filter	Δt _{2GD VOUT3}	to 4.43MHz		6	20	ns
VOUT3 Group delay deviation 3	with filter	Δt _{3GD VOUT3}	to 6MHz		13	20	ns
VOUT3 Crosstalk	CT _{VOUT3}	SIN wave : 1V f=4.43MHz		-60	-55	dB	

Note2 : VCA Level linearity error 1LSB=(G_{VVCAmax}-G_{VVCAmin})/255

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
YOUT3 (67pin) electrical characteristics							
YOUT3 Voltage gain	G _{VYOUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB	
YOUT3 Frequency characteristic	with filter	f _{1YOUT3}	SIN wave : 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f _{2YOUT3}	SIN wave : 1V 27MHz/100kHz		-33.0	-24.0	dB
YOUT3 Input dynamic range	DR _{YOUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V	
YOUT3 Group delay	with filter	t _{GD YOUT3}	at 100kHz		55	ns	
YOUT3 Group delay deviation 1	with filter	Δt _{1GD YOUT3}	to 3.58MHz		4	20	ns
YOUT3 Group delay deviation 2	with filter	Δt _{2GD YOUT3}	to 4.43MHz		6	20	ns
YOUT3 Group delay deviation 3	with filter	Δt _{3GD YOUT3}	to 6MHz		13	20	ns
YOUT3 Crosstalk	CT _{YOUT3}	SIN wave : 1V f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
COOUT3(63pin) electrical characteristics							
COOUT3 Voltage gain	G _{VCOUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB	
COOUT3 Frequency characteristic	with filter	f _{1COOUT3}	SIN wave : 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f _{2COOUT3}	SIN wave : 1V 27MHz/100kHz		-33.0	-24.0	dB
COOUT3 Input dynamic range	DR _{COOUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V	
COOUT3 Group delay	with filter	t _{GD COOUT3}	at 100kHz		55	ns	
COOUT3 Group delay deviation 1	with filter	Δt _{1GD COOUT3}	to 3.58MHz		4	20	ns
COOUT3 Group delay deviation 2	with filter	Δt _{2GD COOUT3}	to 4.43MHz		6	20	ns
COOUT3 Group delay deviation 3	with filter	Δt _{3GD COOUT3}	to 6MHz		13	20	ns
COOUT3 Crosstalk	CT _{COOUT3}	SIN wave : 1V f=4.43MHz		-60	-55	dB	
CYOUT1(75pin) electrical characteristics							
CYOUT1 Voltage gain	G _{VCYOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB	
CYOUT1 Frequency characteristic Peak	f _{peakCYOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB	
CYOUT1 Frequency characteristic	without filter	f _{1CYOUT1}	0.3V SYNC+0.7V SIN wave 100MHz/100kHz	-3.0	-1.0	1.0	dB
	with filter1	f _{11CYOUT1}	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{12CYOUT1}	0.3V SYNC+0.7V SIN wave 27MHz/100kHz		-55.0	-50.0	dB
	with filter2	f _{21CYOUT1}	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{22CYOUT1}	0.3V SYNC+0.7V SIN wave 54MHz/100kHz		-55.0	-50.0	dB
	with filter3	f _{31CYOUT1}	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{32CYOUT1}	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		-35.0	-25.0	dB
CYOUT1 Input dynamic range	DR _{CYOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
CYOUT1 (75pin) electrical characteristics							
CYOUT1 Group delay	with filter1	t1GD CYOUT1	at 100kHz		80	ns	
	with filter2	t2GD CYOUT1	at 100kHz		45	ns	
	with filter3	t3GD CYOUT1	at 100kHz		25	ns	
CYOUT1 Group delay deviation 11	with filter1	Δ t1GD CYOUT1	to 3.58MHz		4	20	ns
CYOUT1 Group delay deviation 12		Δ t12GD CYOUT1	to 4.43MHz		6	20	ns
CYOUT1 Group delay deviation 13		Δ t13GD CYOUT1	to 6MHz		15	30	ns
CYOUT1 Group delay deviation 21	with filter2	Δ t21GD CYOUT1	to 3.58MHz		4	20	ns
CYOUT1 Group delay deviation 22		Δ t22GD CYOUT1	to 4.43MHz		6	20	ns
CYOUT1 Group delay deviation 23		Δ t23GD CYOUT1	to 12MHz		15	30	ns
CYOUT1 Group delay deviation 31	with filter3	Δ t31GD CYOUT1	to 3.58MHz		1	20	ns
CYOUT1 Group delay deviation 32		Δ t32GD CYOUT1	to 4.43MHz		1	20	ns
CYOUT1 Group delay deviation 33		Δ t33GD CYOUT1	to 24MHz		5	20	ns
CYOUT1 Crosstalk	CTCYOUT1	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
PbOUT1 (74pin) electrical characteristics							
PbOUT1 Voltage gain	G _{VPbOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB	
PbOUT1 Frequency characteristic Peak	f _{peakPbOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB	
PbOUT1 Frequency characteristic	without filter	f _{1PbOUT1}	0.3V SYNC+0.7V SIN wave 100MHz/100kHz	-3.0	-1.0	1.0	dB
	with filter1	f _{11PbOUT1}	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{12PbOUT1}	0.3V SYNC+0.7V SIN wave 27MHz/100kHz		-55.0	-50.0	dB
	with filter2	f _{21PbOUT1}	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{22PbOUT1}	0.3V SYNC+0.7V SIN wave 54MHz/100kHz		-55.0	-50.0	dB
	with filter3	f _{31PbOUT1}	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz	-3.0	-1.0	1.0	dB
		f _{32PbOUT1}	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		-35.0	-25.0	dB
PbOUT1 Input dynamic range	DR _{PbOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V	
PbOUT1 Group delay	with filter1	t _{1GD PbOUT1}	at 100kHz		80		ns
	with filter2	t _{2GD PbOUT1}	at 100kHz		45		ns
	with filter3	t _{3GD PbOUT1}	at 100kHz		25		ns
PbOUT1 Group delay deviation 11	with filter1	Δt _{11GD PbOUT1}	to 3.58MHz		4	20	ns
PbOUT1 Group delay deviation 12		Δt _{12GD PbOUT1}	to 4.43MHz		6	20	ns
PbOUT1 Group delay deviation 13		Δt _{13GD PbOUT1}	to 6MHz		15	30	ns

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
PbOUT1 (74pin) electrical characteristics							
PbOUT1 Group delay deviation 21	with filter2	$\Delta t_{21GD PbOUT1}$	to 3.58MHz		4	20 ns	
PbOUT1 Group delay deviation 22		$\Delta t_{22GD PbOUT1}$	to 4.43MHz		6	20 ns	
PbOUT1 Group delay deviation 23		$\Delta t_{23GD PbOUT1}$	to 12MHz		15	30 ns	
PbOUT1 Group delay deviation 31	with filter3	$\Delta t_{31GD PbOUT1}$	to 3.58MHz		1	20 ns	
PbOUT1 Group delay deviation 32		$\Delta t_{32GD PbOUT1}$	to 4.43MHz		1	20 ns	
PbOUT1 Group delay deviation 33		$\Delta t_{33GD PbOUT1}$	to 24MHz		5	20 ns	
PbOUT1 Crosstalk	CT_{PbOUT1}	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB	
PrOUT1 (73pin) electrical characteristics							
PrOUT1 Voltage gain	$G_{VP-OUT1}$	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB	
PrOUT1 Frequency characteristic Peak	$f_{peakPrOUT1}$	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB	
PrOUT1 Frequency characteristic	without filter	$f_{1PrOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		-3.0	-1.0	1.0 dB
	with filter1	$f_{11PrOUT1}$	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz		-3.0	-1.0	1.0 dB
		$f_{12PrOUT1}$	0.3V SYNC+0.7V SIN wave 27MHz/100kHz			-55.0	-50.0 dB
	with filter2	$f_{21PrOUT1}$	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz		-3.0	-1.0	1.0 dB
		$f_{22PrOUT1}$	0.3V SYNC+0.7V SIN wave 54MHz/100kHz			-55.0	-50.0 dB
	with filter3	$f_{31PrOUT1}$	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz		-3.0	-1.0	1.0 dB
		$f_{32PrOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz			-35.0	-25.0 dB
PrOUT1 Input dynamic range	DR_{PrOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
PrOUT1 (73pin) electrical characteristics							
PrOUT1 Group delay	with filter1	t1 _{GD PrOUT1}	at 100kHz		80	ns	
	with filter2	t2 _{GD PrOUT1}	at 100kHz		45	ns	
	with filter3	t3 _{GD PrOUT1}	at 100kHz		25	ns	
PrOUT1 Group delay deviation 11	with filter1	Δt1 _{GD PrOUT1}	to 3.58MHz		4	20	ns
PrOUT1 Group delay deviation 12		Δt12 _{GD PrOUT1}	to 4.43MHz		6	20	ns
PrOUT1 Group delay deviation 13		Δt13 _{GD PrOUT1}	to 6MHz		15	30	ns
PrOUT1 Group delay deviation 21	with filter2	Δt21 _{GD PrOUT1}	to 3.58MHz		4	20	ns
PrOUT1 Group delay deviation 22		Δt22 _{GD PrOUT1}	to 4.43MHz		6	20	ns
PrOUT1 Group delay deviation 23		Δt23 _{GD PrOUT1}	to 12MHz		15	30	ns
PrOUT1 Group delay deviation 31	with filter3	Δt31 _{GD PrOUT1}	to 3.58MHz		1	20	ns
PrOUT1 Group delay deviation 32		Δt32 _{GD PrOUT1}	to 4.43MHz		1	20	ns
PrOUT1 Group delay deviation 33		Δt33 _{GD PrOUT1}	to 30MHz		12	20	ns
PrOUT1 Crosstalk	CT _{PrOUT1}	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CYOUT2 (71pin) electrical characteristics						
CYOUT2 Voltage gain	G _{VCYOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB
CYOUT2 Frequency characteristic Peak	f _{peakCYOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
CYOUT2 Frequency characteristic	f _{1CYOUT2}	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	-3.0	-1.0	0.0	dB
CYOUT2 Input dynamic range	DR _{CYOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
CYOUT2 Crosstalk	CT _{CYOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB
PbOUT2 (70pin) electrical characteristics						
PbOUT2 Voltage gain	G _{VPbOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB
PbOUT2 Frequency characteristic Peak	f _{peakPbOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
PbOUT2 Frequency characteristic	f _{1PbOUT2}	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	-3.0	-1.0	0.0	dB
PbOUT2 Input dynamic range	DR _{PbOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
PbOUT2 Crosstalk	CT _{PbOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB
PrOUT2 (69pin) electrical characteristics						
PrOUT2 Voltage gain	G _{VPrOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	-0.3	0.0	0.3	dB
PrOUT2 Frequency characteristic Peak	f _{peakPrOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
PrOUT2 Frequency characteristic	f _{1PrOUT2}	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	-3.0	-1.0	0.0	dB
PrOUT2 Input dynamic range	DR _{PrOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
PrOUT2 Crosstalk	CT _{PrOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		-60	-55	dB
Group delay deviation between each channels (OUT1~OUT3)						
Group delay deviation between C and Y	Δt_{1chGD}	between C and Y at 3.58MHz		0	10	ns
Group delay deviation between CY and Pb (Pr)	Δt_{2chGD}	between CY and Pb (Pr) at 8MHz		0	10	ns

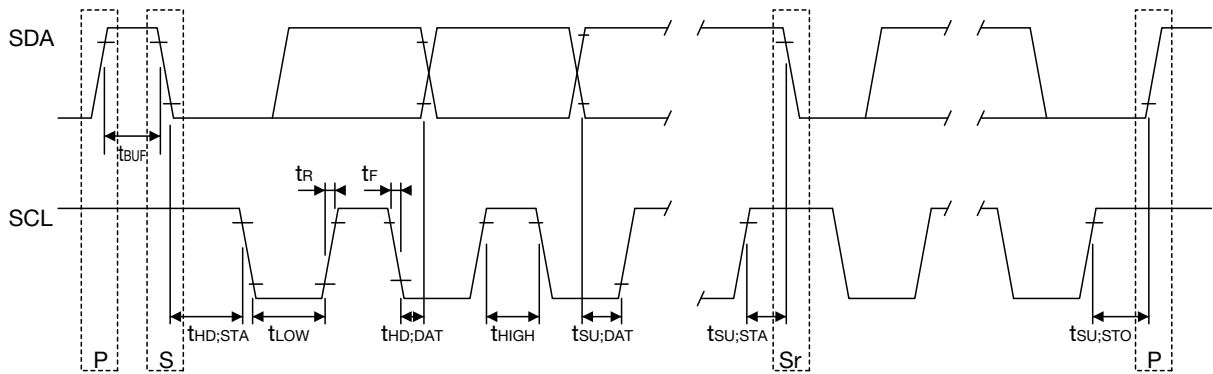
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
L,ROUT (34~39pin) electrical characteristics								
L,ROUT Voltage gain	0dB	Gv1L, ROUT	SIN wave : 1Vrms f=1kHz		-0.3	0.0	0.3	dB
	6dB	Gv2 L, ROUT	SIN wave : 1Vrms f=1kHz		5.7	6.0	6.3	dB
L,ROUT Frequency characteristic	0dB	f1L, ROUT	SIN wave : 1Vrms f=50kHz		-3.0			dB
	6dB	f2L, ROUT	SIN wave : 1Vrms f=50kHz		-3.0			dB
Total harmonic distortion	THD	SIN wave : 1Vrms f=1kHz, Gv=0dB			0.03	0.05	%	
Input dynamic range	DR	f=1kHz, THD=0.5% Gv=0dB		2.8	3.0		Vrms	
Crosstalk	CT	SIN wave 1Vrms f=1kHz			-90	-80	dB	
Ripple rejection	PSRR	Vcc = 9V+0.1Vrms (SIN wave) at 100Hz			-50	-40	dB	
Output offset voltage	V _{OFF1}	DC offset at the switching time, Gv=0dB		-15	0	15	mV	
	V _{OFF2}	DC offset at the switching time, Gv=6dB		-30	0	30		
S/N ratio	S/N1	1kHz, A curve, 1Vrms Gv=0dB			-90	-80	dB	
	S/N2	1kHz, A curve, 1Vrms Gv=6dB			-80	-70	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
O1 (5pin) electrical characteristics						
O1 pin low level output voltage	V _{O1}	O1 pin sink 5mA	GND		0.4	V
O1 pin Leak current (at the time of OFF)	I _{O1}	O1=5.0V	-10		10	μA
O2 (17pin) electrical characteristics						
O2 pin low level output voltage	V _{O2}	O2 pin sink 5mA	GND		0.4	V
O2 pin Leak current (at the time of OFF)	I _{O2}	O2=5.0V	-10		10	μA
O3 (23pin) electrical characteristics						
O3 pin low level output voltage	V _{O3}	O3 pin sink 5mA	GND		0.4	V
O3 pin Leak current (at the time of OFF)	I _{O3}	O3=5.0V	-10		10	μA
FLAG (29pin) electrical characteristics						
FLAG pin low level output voltage	V _{FLAG}	FLAG pin sink 5mA	GND		0.4	V
FLAG pin Leak current (at the time of OFF)	I _{FLAG}	FLAG=5.0V	-10		10	μA
DL1 (81,87,93pin) electrical characteristics						
DL1 Input Voltage	Low	V _{LDL1}	GND		1.0	V
	Middle	V _{MDL1}	1.3		2.7	V
	High	V _{HDL1}	3.5		V _{CC5}	V
DL2 (83,89,95pin) electrical characteristics						
DL2 Input Voltage	Low	V _{LDL2}	GND		2.7	V
	High	V _{HDL2}	3.5		V _{CC5}	V
DL3 (85,91,97pin) electrical characteristics						
DL3 Input Voltage	Low	V _{LDL3}	GND		1.0	V
	Middle	V _{MDL3}	1.3		2.7	V
	High	V _{HDL3}	3.5		V _{CC5}	V

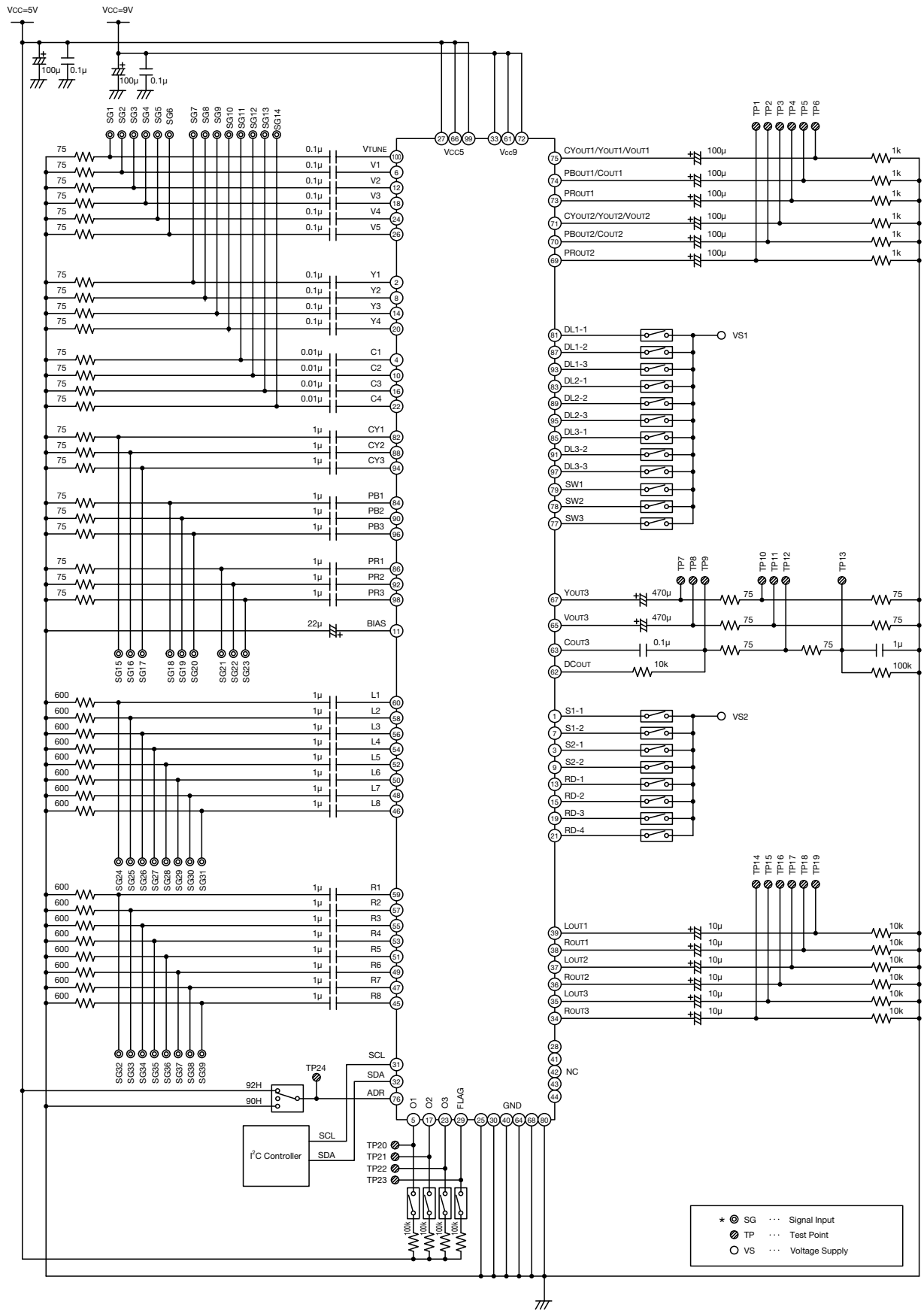
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
SW (79,78,77pin) electrical characteristics								
SW Input Voltage	Low	V_{LSW}	GND		2.0	V		
	High	V_{HSW}	3.0		Vcc5	V		
SW output current at terminal voltage "Low"		I_{SW}	SW=GND		19	27	35	μ A
S2 (3,9pin) electrical characteristics								
S2 Input Voltage1	Low	$V_{LS2/FS}$	GND		1.0	V		
	Middle	$V_{MS2/FS}$	S, D-Detect Mode		1.3		2.7	V
	High	$V_{HS2/FS}$	3.5		Vcc5	V		
S1 (1,7rpin) electrical characteristics								
S1 Input Voltage	Low	V_{LS1}	GND		2.0	V		
	High	V_{HS1}	3.0		Vcc5	V		
S1 output current at terminal voltage "Low"		I_{S1}	S1=GND		19	27	35	μ A
ADR (76pin) electrical characteristics								
ADR Input Voltage	Low	V_{LADR}	90H select		GND		0.8	V
	High	V_{HADR}	92H select		2.5		Vcc5	V
ADR input current at terminal voltage "High"		I_{ADR}	ADR=5.0V		50	70	90	μ A
RD (13,15,19,21pin) electrical characteristics								
RD Input Voltage	Low	V_{LRD}	GND		2.0	V		
	High	V_{HRD}	3.0		Vcc5	V		
RD output current at terminal voltage "Low"		I_{RD}	RD=GND		19	27	35	μ A

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I ² C condition (note3)						
Input voltage L	V _{IL}		GND		0.8	V
Input voltage H	V _{IH}		2.2		V _{CC5}	V
SDA low level output voltage	V _{OL}	SDA sink 3mA	GND		0.4	V
High level input current	I _{IH}	SDA, SCL=4.5V	-10		10	μA
Low level input current	I _{IL}	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f _{SCL}				400	kHz
Data transfer wait time	t _{BUF}		1.3			μs
SCL start hold time	t _{HD;STA}		0.6			μs
SCL low level hold time	t _{LOW}		1.3			μs
SCL high level hold time	t _{HIGH}		0.6			μs
Start condition setup time	t _{SU;STA}		0.6			μs
SDA data hold time	t _{HD;DAT}		0			μs
SDA data setup time	t _{SU;DAT}		100			ns
SDA,SCL rise time	t _R				300	ns
SDA,SCL fall time	t _F				300	ns
Stop condition setup time	t _{SU;STO}		0.6			μs

Note 3 : I²C condition



Measuring Circuit



■ Table of control registers

No.	DATA condition							
	b07	b06	b05	b04	b03	b02	b01	b00
DATA1 [00H]	OUT1 LPF select		OUT1 Power Save	X	OUT1 LINE SELECT			
	X	X	OUT2 Power Save	X	OUT2 LINE SELECT			
DATA3 [00H]	DCout Voltage		OUT3 Power Save	X	OUT3 LINE SELECT			
	Audio OUT1 LINE SELECT				Audio OUT2 LINE SELECT			
DATA5 [00H]	X	AO1 GAIN SW	AO2 GAIN SW	AO3 GAIN SW	Audio OUT3 LINE SELECT			
	X	AO1 Power Save	AO2 Power Save	AO3 Power Save	O1	O2	O3	X
DATA7 [00H]	VCA GAIN SELECT							

* [00H] is in the initial state of control registers.

■ Details of the contents of control (1)

OUT1 LINE SELECT

b03	b02	b01	b00	CYout1 (75pin)	PBout1 (74pin)	PRout1 (73pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V _{TUNE}	Mute	Mute
0	0	1	0	V1	Mute	Mute
0	0	1	1	V2	Mute	Mute
0	1	0	0	V3	Mute	Mute
0	1	0	1	V4	Mute	Mute
0	1	1	0	V5	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

OUT2 LINE SELECT

b13	b12	b11	b10	CYout2 (71pin)	PBout2 (70pin)	PRout2 (69pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V _{TUNE}	Mute	Mute
0	0	1	0	V1	Mute	Mute
0	0	1	1	V2	Mute	Mute
0	1	0	0	V3	Mute	Mute
0	1	0	1	V4	Mute	Mute
0	1	1	0	V5	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

■ Details of the contents of control (2)

OUT3 LINE SELECT

(*1)

b23	b22	b21	b20	Vout3 (65pin)	Yout3 (67pin)	Cout3 (63pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Y1+C1	Y1	C1
0	0	1	0	Y2+C2	Y2	C2
0	0	1	1	Y3+C3	Y3	C3
0	1	0	0	Y4+C4	Y4	C4
0	1	0	1	Mute	Mute	Mute
0	1	1	0	Mute	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Mute	Mute	Mute
1	0	0	1	V _{TUNE}	Mute	Mute
1	0	1	0	V1	Mute	Mute
1	0	1	1	V2	Mute	Mute
1	1	0	0	V3	Mute	Mute
1	1	0	1	V4	Mute	Mute
1	1	1	0	V5	Mute	Mute
1	1	1	1	Mute	Mute	Mute

(*1) When DCout is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

LPF Cutoff Frequency Select

OUT1 (73,74,75pin)

b07	b06	LPF fc
0	0	through
0	1	37.5MHz
1	0	13.5MHz
1	1	6.75MHz

Powersave

OUT1 (73,74,75pin)

b05	Conditions
0	Active
1	PowerSave

OUT2 (69,70,71pin)

b15	Conditions
0	Active
1	PowerSave

OUT3 (63,65,67pin)

b25	Conditions
0	Active
1	PowerSave

OUTPUT PORT Control

O1 (5pin)

b53	Conditions
0	Low
1	Open

O2 (17pin)

b52	Conditions
0	Low
1	Open

O3 (23pin)

b51	Conditions
0	Low
1	Open

DCout (62pin) OUTPUT VOLTAGE

b27	b26	VOLTAGE
0	0	0V
0	1	2.2V
1	0	5V
1	1	Hi-Impedance (*2)

(*2) When DCout is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

■ Details of the contents of control (3)

VCA GAIN SELECT

b67	b66	b65	b64	b63	b62	b61	b60	Hex	Dec	Gv(*3) [V]	Gv[dB]
0	0	0	0	0	0	0	0	00	00	0.500	-6.02
0	0	0	0	0	0	0	1	01	01	0.505	-5.94
0	0	0	0	0	0	1	0	02	02	0.510	-5.85
0	0	0	0	0	0	1	1	03	03	0.515	-5.77
0	0	0	0	0	1	0	0	04	04	0.520	-5.69
0	0	0	0	0	1	0	1	05	05	0.525	-5.60
0	0	0	0	0	1	1	0	06	06	0.529	-5.52
0	0	0	0	0	1	1	1	07	07	0.534	-5.44
0	0	0	0	1	0	0	0	08	08	0.539	-5.36
0	0	0	0	1	0	0	1	09	09	0.544	-5.29
0	0	0	0	1	0	1	0	0A	10	0.549	-5.21
0	0	0	0	1	0	1	1	0B	11	0.554	-5.13
0	0	0	0	1	1	0	0	0C	12	0.559	-5.05
0	0	0	0	1	1	0	1	0D	13	0.564	-4.98
0	0	0	0	1	1	1	0	0E	14	0.569	-4.90
0	0	0	0	1	1	1	1	0F	15	0.574	-4.83
0	1	0	1	1	1	1	0	5E	94	0.961	-0.35
0	1	0	1	1	1	1	1	5F	95	0.966	-0.30
0	1	1	0	0	0	0	0	60	96	0.971	-0.26
0	1	1	0	0	0	0	1	61	97	0.975	-0.22
0	1	1	0	0	0	1	0	62	98	0.980	-0.17
0	1	1	0	0	0	1	1	63	99	0.985	-0.13
0	1	1	0	0	1	0	0	64	100	0.990	-0.09
0	1	1	0	0	1	0	1	65	101	0.995	-0.04
0	1	1	0	0	1	1	0	66	102	1.000	0.00
0	1	1	0	0	1	1	1	67	103	1.005	0.04
0	1	1	0	1	0	0	0	68	104	1.010	0.08
0	1	1	0	1	0	0	1	69	105	1.015	0.13
0	1	1	0	1	0	1	0	6A	106	1.020	0.17
0	1	1	0	1	0	1	1	6B	107	1.025	0.21
0	1	1	0	1	1	0	0	6C	108	1.029	0.25
0	1	1	0	1	1	0	1	6D	109	1.034	0.29
1	1	1	1	0	0	0	0	F0	240	1.676	4.49
1	1	1	1	0	0	0	1	F1	241	1.681	4.51
1	1	1	1	0	0	1	0	F2	242	1.686	4.54
1	1	1	1	0	0	1	1	F3	243	1.691	4.56
1	1	1	1	0	1	0	0	F4	244	1.696	4.59
1	1	1	1	0	1	0	1	F5	245	1.701	4.61
1	1	1	1	0	1	1	0	F6	246	1.706	4.64
1	1	1	1	0	1	1	1	F7	247	1.711	4.66
1	1	1	1	1	0	0	0	F8	248	1.716	4.69
1	1	1	1	1	0	0	1	F9	249	1.721	4.71
1	1	1	1	1	0	1	0	FA	250	1.725	4.74
1	1	1	1	1	0	1	1	FB	251	1.730	4.76
1	1	1	1	1	1	0	0	FC	252	1.735	4.79
1	1	1	1	1	1	0	1	FD	253	1.740	4.81
1	1	1	1	1	1	1	0	FE	254	1.745	4.84
1	1	1	1	1	1	1	1	FF	255	1.750	4.86

(*3) $Gv = V_{out}(VTUNE=Vin1+1V) - V_{out}(VTUNE=Vin1)$ at 71,75 pin

$$Gv = 0.50 + (1.25/255) * 'Dec'$$

Above Gv is a design theoretical value.

■ Details of the contents of control (4)

Audio OUT1 LINE SELECT

b37	b36	b35	b34	Lout1 (39pin)	Rout1 (38pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT2 LINE SELECT

b33	b32	b31	b30	Lout2 (37pin)	Rout2 (36pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT3 LINE SELECT

b43	b42	b41	b40	Lout3 (35pin)	Rout3 (34pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

■ **Details of the contents of control (5)**

Audio GAIN SW

OUT1 (38,39pin)

b46	GAIN
0	0dB
1	6dB

OUT2 (36,37pin)

b45	GAIN
0	0dB
1	6dB

OUT3 (34,35pin)

b44	GAIN
0	0dB
1	6dB

Audio Powersave

OUT1 (38,39pin)

b56	Conditions
0	Active
1	PowerSave

OUT2 (36,37pin)

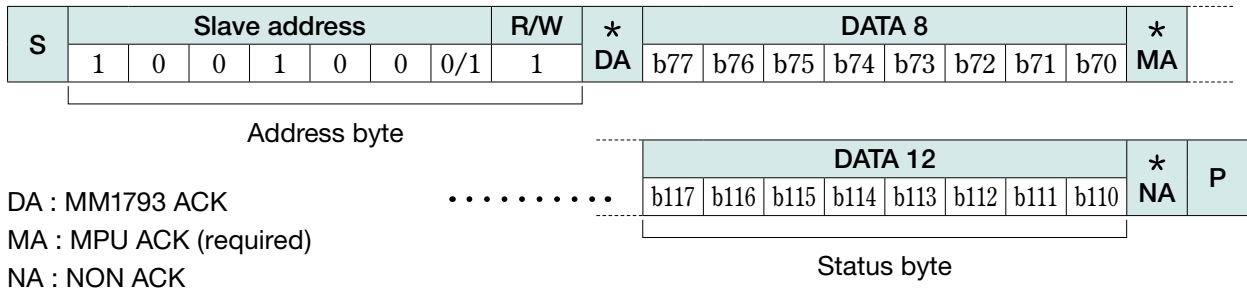
b55	Conditions
0	Active
1	PowerSave

OUT3 (34,35pin)

b54	Conditions
0	Active
1	PowerSave

Status registers

Status registers are data to inform the master of the device status.
The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers.

As MM1793 slave address, either 91H or 93H can be selected according to the ADR terminal conditions. When ADR terminal is L, 91H is selected.

Set the confirmation acknowledgement after the end of status register to non-ACK.

The following figure shows the correspondence of the output data of status registers.

Table of status registers (*2)

No.	DATA condition							
	b77	b76	b75	b74	b73	b72	b71	b70
DATA8	X	X	SW1 DETECT	DL1-1 DETECT		DL2-1 DETECT	DL3-1 DETECT	
DATA9	X	X	SW2 DETECT	DL1-2 DETECT		DL2-2 DETECT	DL3-2 DETECT	
DATA10	X	X	SW3 DETECT	DL1-3 DETECT		DL2-3 DETECT	DL3-3 DETECT	
DATA11	X	X	S1-1 DETECT	S2-1 DETECT		S1-2 DETECT	S2-2 DETECT	
DATA12	X	X	RD-1 DETECT	X	RD-2 DETECT	RD-3 DETECT	X	RD-4 DETECT

(*2) Control registers (DATA1 to DATA7) are not affected when reading status registers (DATA8 to DATA12).

■ Output data of status registers & threshold (1)

It is based on CPR1202 which is the specification of JEITA.
(Except where noted otherwise, Ta=25°C, Vcc9=9V, Vcc5=5V)

S1-1~S1-2 (1,7,pin) DETECT

S1-1~S1-2 voltage	Conditions	S1-2	S1-1
		b102	b105
$GND \leq VDC \leq 2.0V$	CONNECTED	1	1
$3.0V \leq VDC \leq V_{cc5}$	UNCONNECTED	0	0

S2-1~S2-2 (3,9pin) DETECT (Aspect)

S2-1~S2-2 voltage	Aspect	S2-2		S2-1	
		b101	b100	b104	b103
$GND \leq VDC \leq 1.0V$	4 : 3	0	0	0	0
$1.3V \leq VDC \leq 2.7V$	Letterbox	0	1	0	1
$3.5V \leq VDC \leq V_{cc5}$	16 : 9	1	0	1	0

DL1-1,DL1-2,DL1-3 (81,87,93pin) DETECT (Scanning Line)

DL1-1~DL1-3 voltage	Scanning Line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
$GND \leq VDC \leq 1.0V$	480	0	0	0	0	0	0
$1.3V \leq VDC \leq 2.7V$	720	0	1	0	1	0	1
$3.5V \leq VDC \leq V_{cc5}$	1080	1	0	1	0	1	0

DL2-1,DL2-2,DL2-3 (83,89,95pin) DETECT (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
$GND \leq VDC \leq 2.7V$	Interlace	0	0	0
$3.5V \leq VDC \leq V_{cc5}$	Progressive	1	1	1

DL3-1,DL3-2,DL3-3 (85,91,97pin) DETECT (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
$GND \leq VDC \leq 1.0V$	4 : 3	0	0	0	0	0	0
$1.3V \leq VDC \leq 2.7V$	Letterbox	0	1	0	1	0	1
$3.5V \leq VDC \leq V_{cc5}$	16 : 9	1	0	1	0	1	0

SW1~SW3 (79,78,77pin) DETECT

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
$GND \leq VDC \leq 2.0V$	CONNECTED	1	1	1
$3.0V \leq VDC \leq V_{cc5}$	UNCONNECTED	0	0	0

RD-1~RD-4 (13,15,19,21pin) DETECT

RD1-1~RD1-4 voltage	Conditions	RD-4	RD-3	RD-2	RD-1
		b110	b112	b113	b115
$GND \leq VDC \leq 2.0V$	UNCONNECTED	0	0	0	0
$3.0V \leq VDC \leq V_{cc5}$	CONNECTED	1	1	1	1

■ The output which monitor and detects a status register

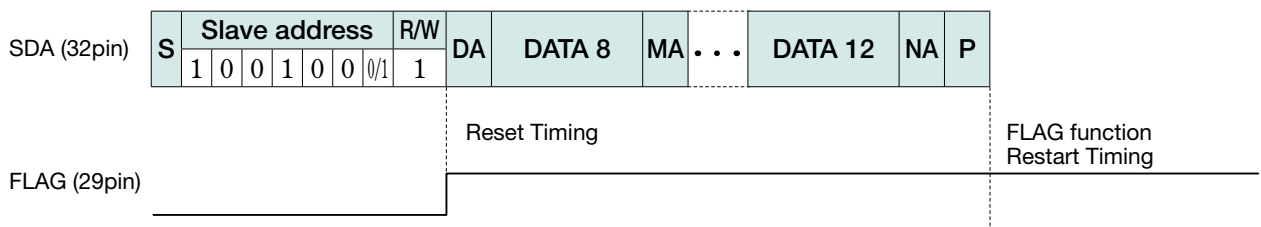
MM1793 is Built-in the function which detects change of a status register and is outputted to a FLAG terminal.

When status register information changes, an output is changed from Open (High) to Low at FLAG terminal. It is the open collector type output port.

Status register information	FLAG (29pin)
change	Low
readed	Open (High)

✧ About Reset of a FLAG terminal (shift to a detection waiting state from a detection state)

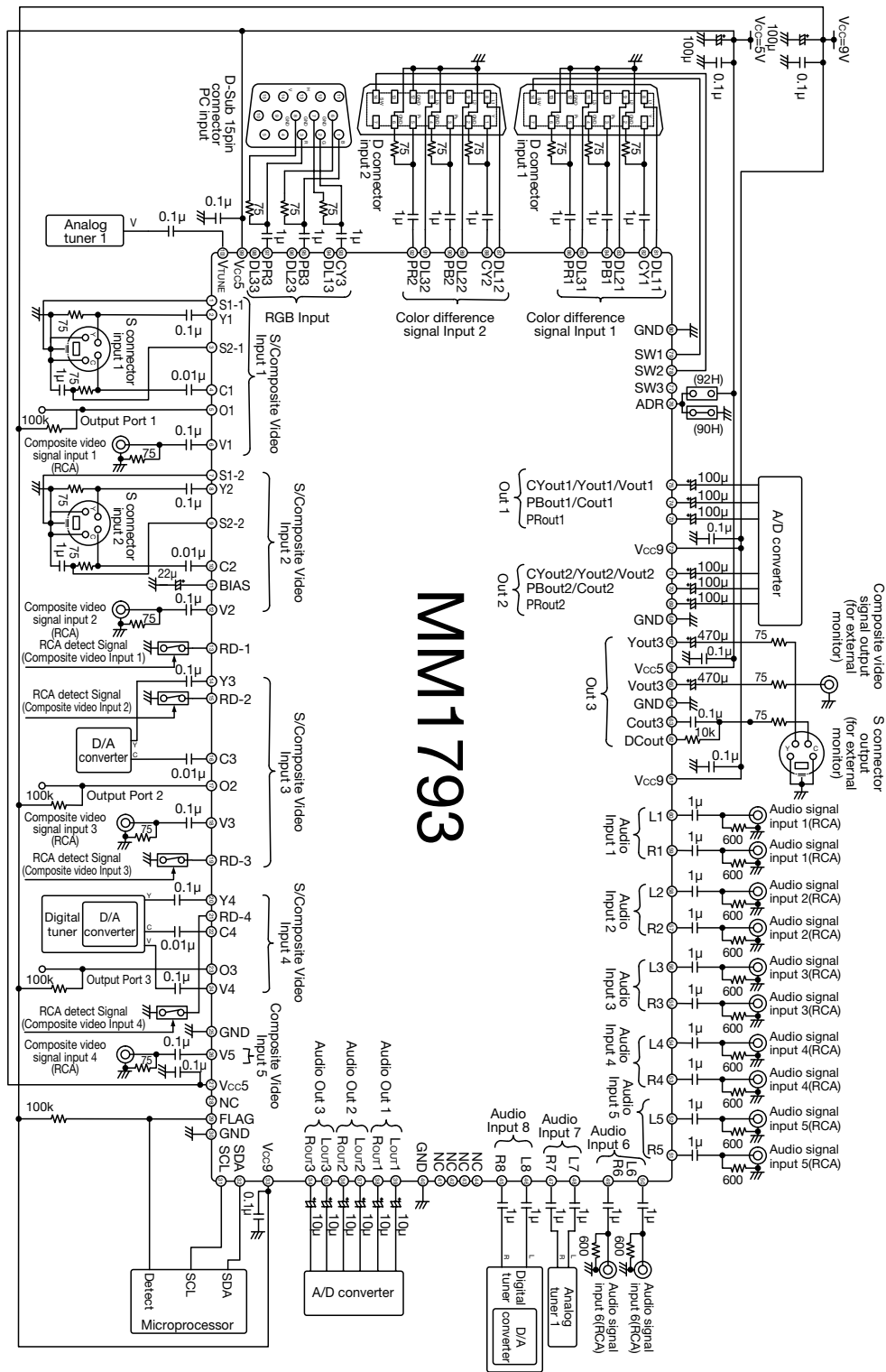
When status register information is readed, an output is changed to Open at FLAG terminal. (Reset) Reset timing from Low to Open (High) of a FLAG terminal is at the R/W bit detection time.



Note : FLAG terminal information does not become fixed by S/D distinction terminal may operate transitionally when power-on. Because, please carry out reading of a status register after a power-on and reset a FLAG terminal.

- Please do not use the interruption function of the master which used the trigger from Low to Open (High) of a FLAG terminal (29Pin).
Because it is reading about a status register at the time of reset timing, the device status may be unable to be normally transmitted to a master
- FLAG functional restart timing is after Stop condition detection of I²C bus.
For the reason, change of the status register between reset timing-Stop Condition is undetectable.
At the time of status register reading which used the FLAG function, please read repeatedly by the master and check the adjustment of a status register.

Application Circuit 1



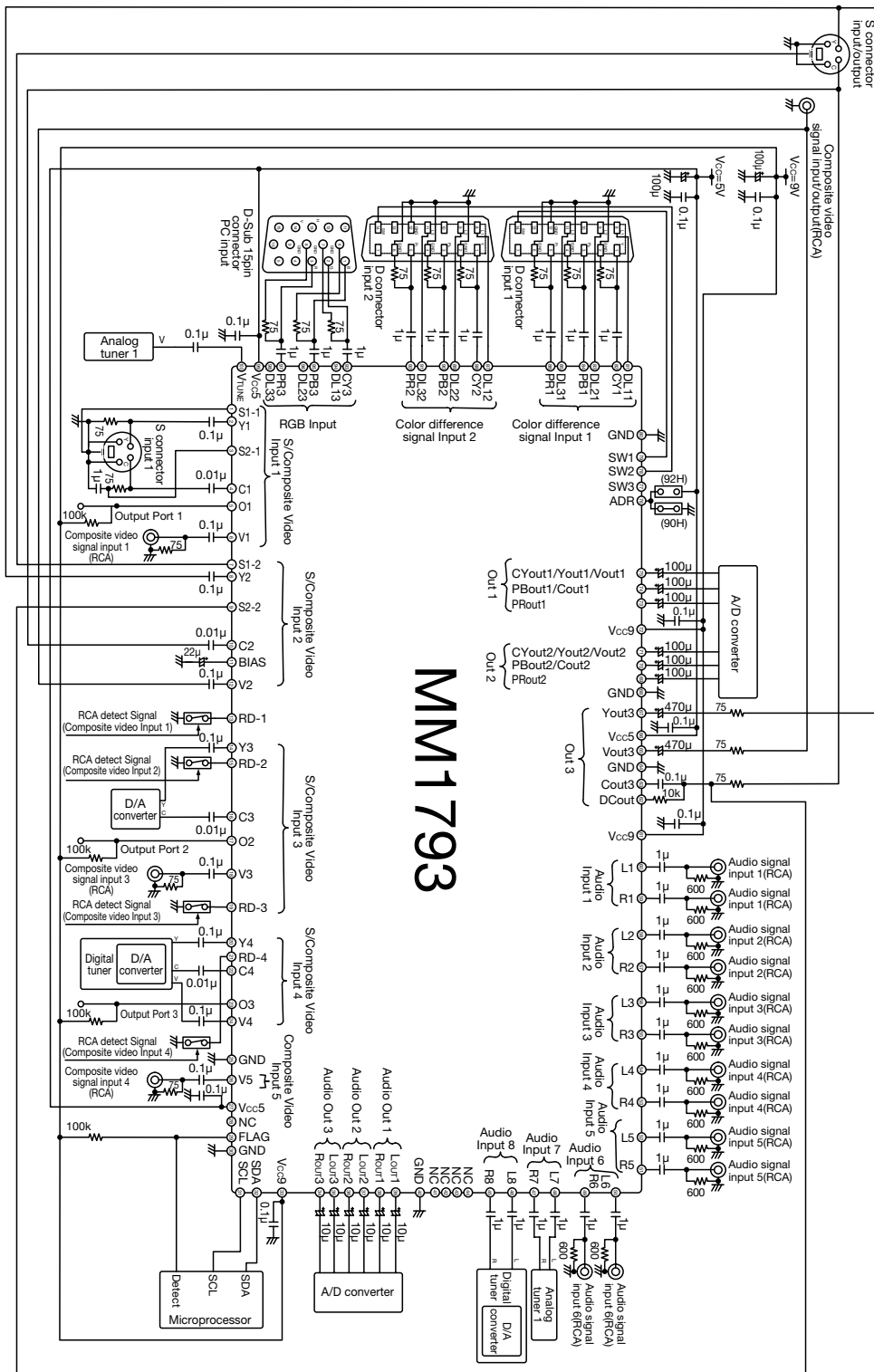
MM1793

Note : Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

We shall not be liable for any trouble or damage caused by using this circuit.

In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

Application Circuit 2



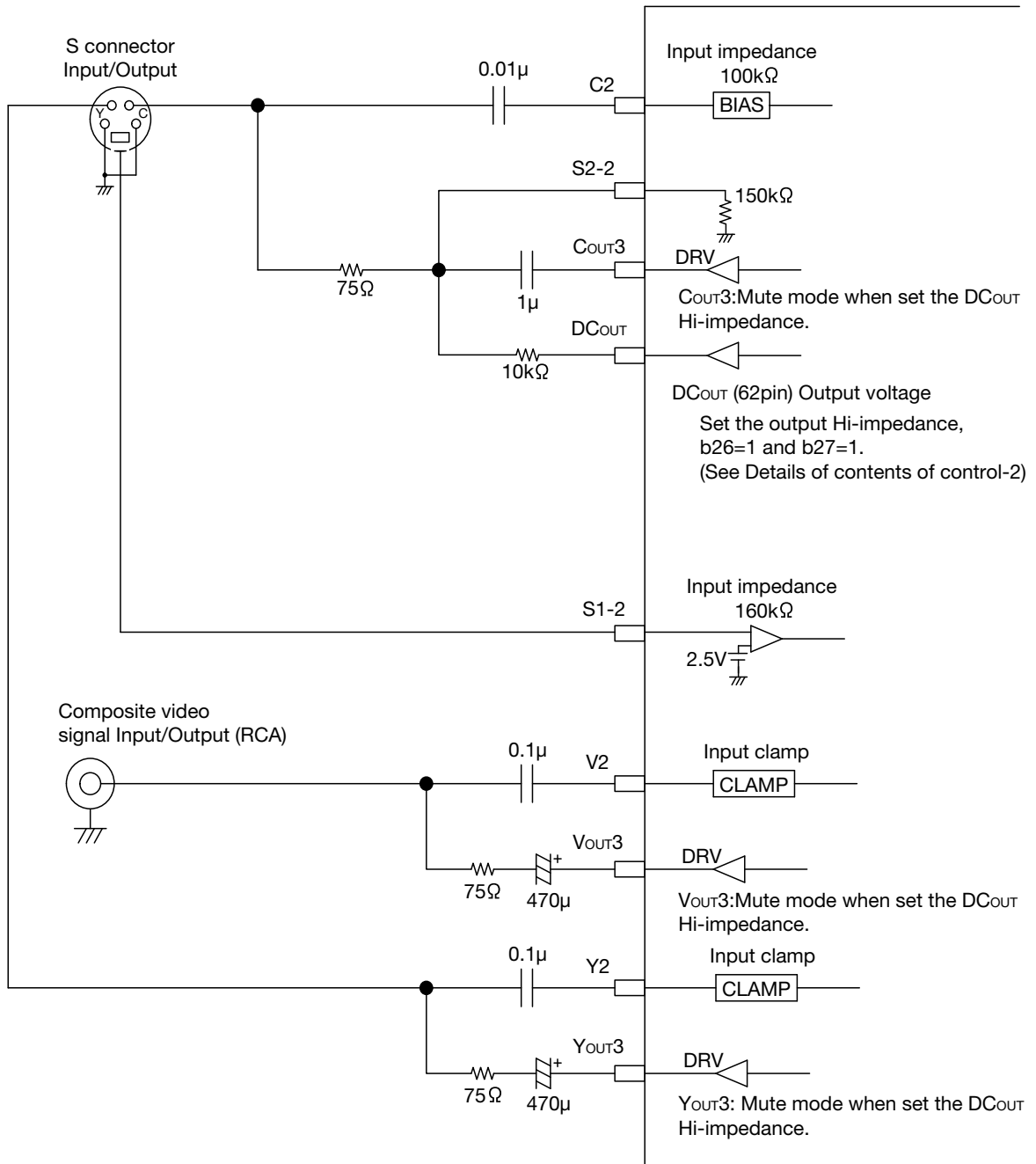
Note : Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

We shall not be liable for any trouble or damage caused by using this circuit.

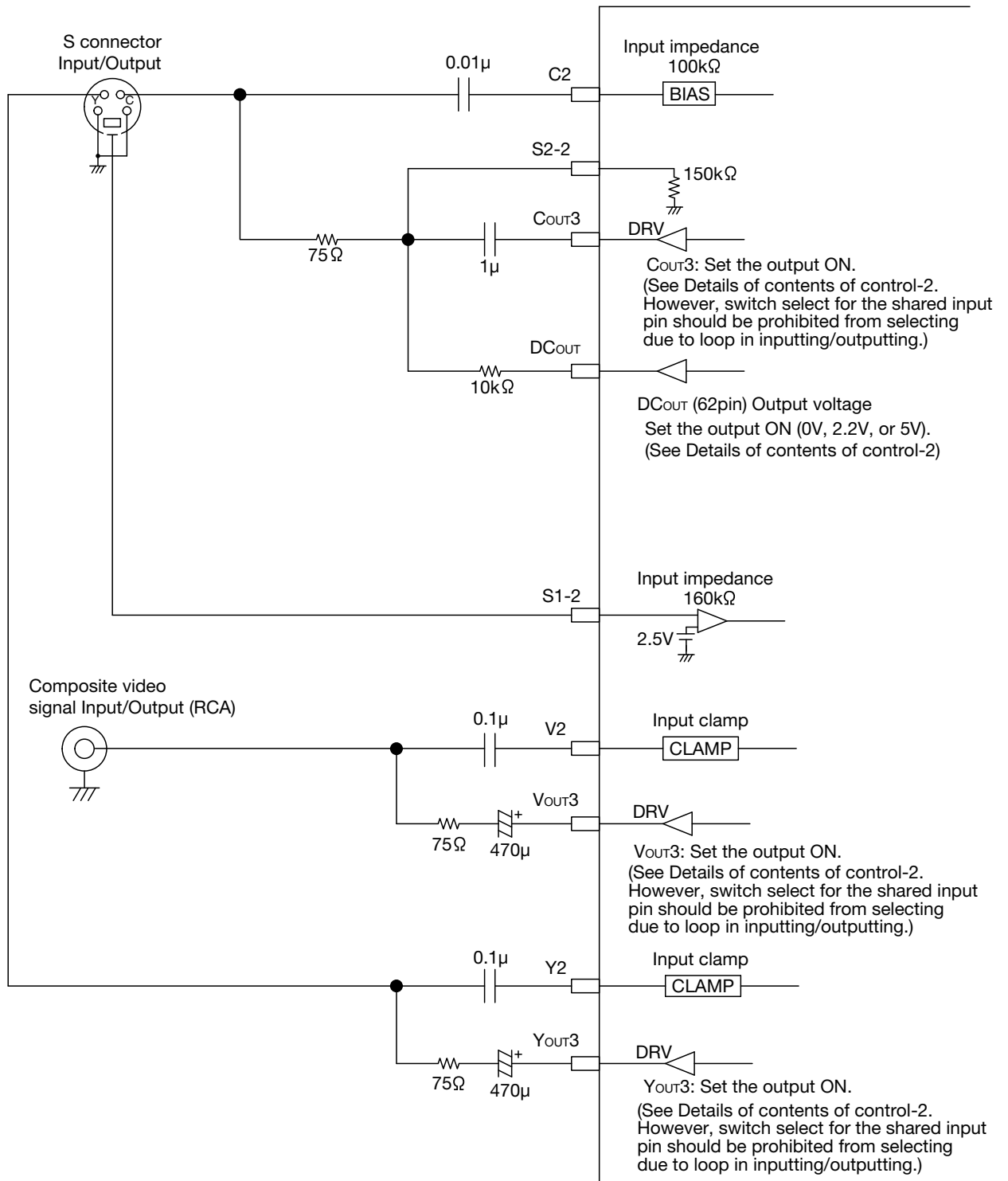
In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

■ Application circuit as an output or an input pin

(1) Settings when used as an input pin

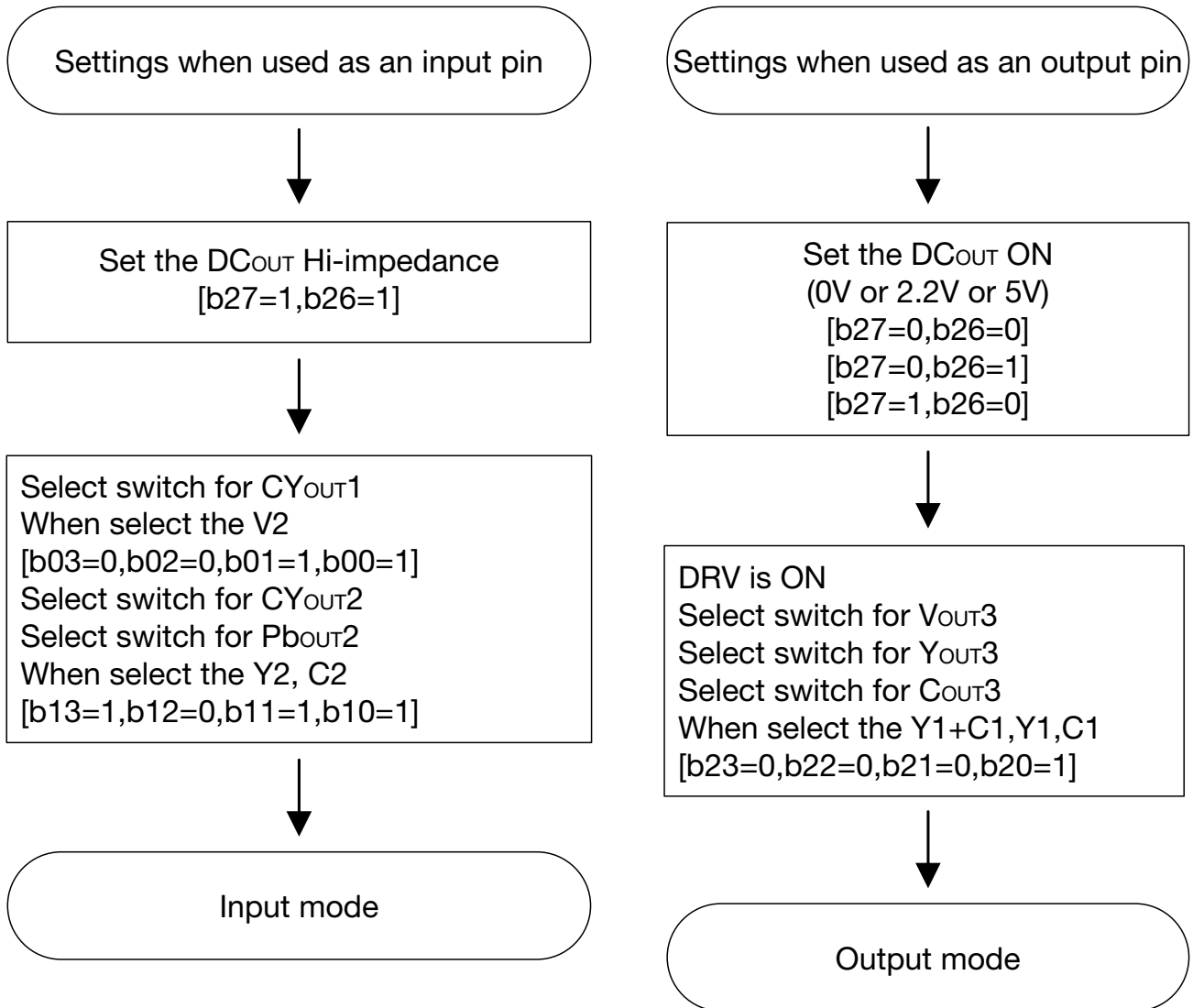


(2) Settings when used as an output pin



■ Applications as an output or an input pin

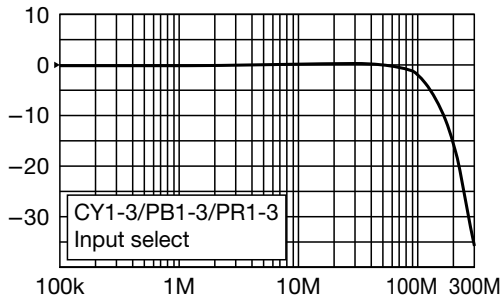
This is a flowchart applying to the Application Circuit2



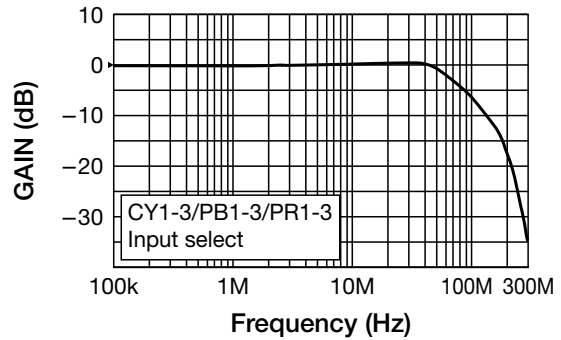
Characteristics (Except where noted otherwise, Ta=25°C, Vcc9=9V, Vcc5=5V, VCA GAIN SELECT='66H')

Frequency characteristic 1

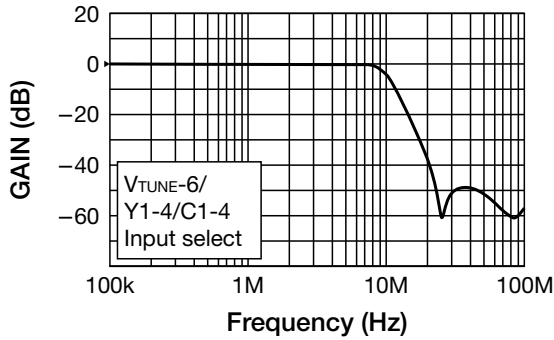
■ OUT1 THRU



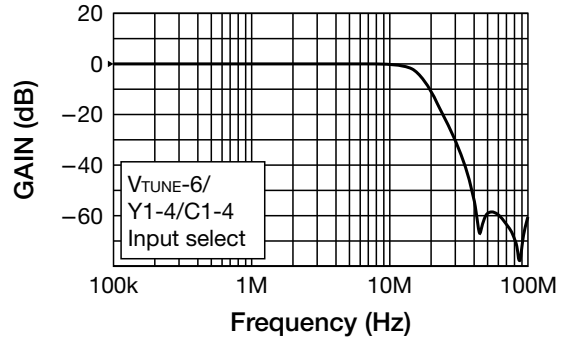
■ OUT2 THRU



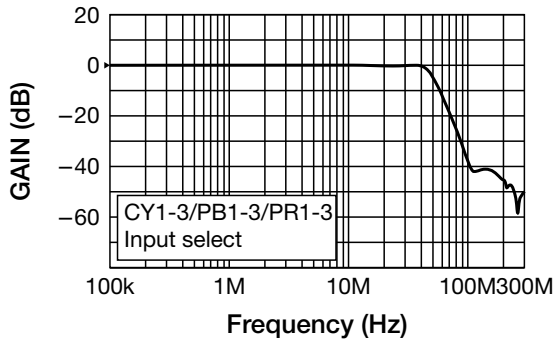
■ OUT1 LPF1 (fc=6.75MHz)



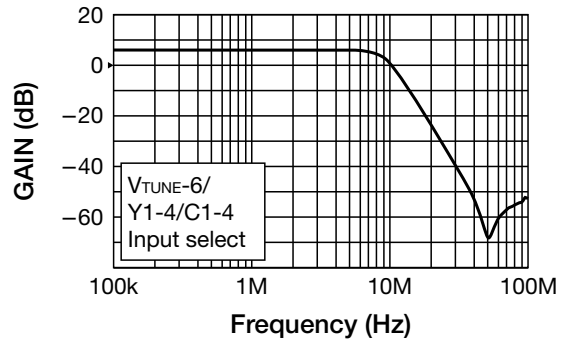
■ OUT1 LPF2 (fc=13.5MHz)



■ OUT1 LPF3 (fc=37.5MHz)

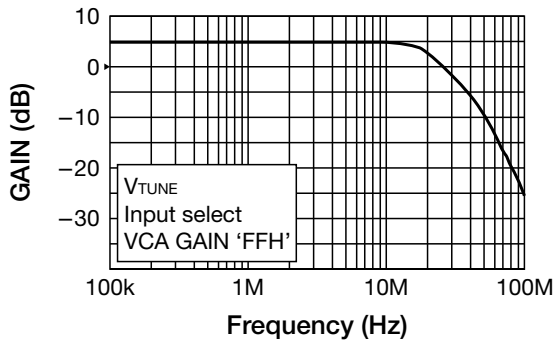


■ OUT3 (fc=6.75MHz)

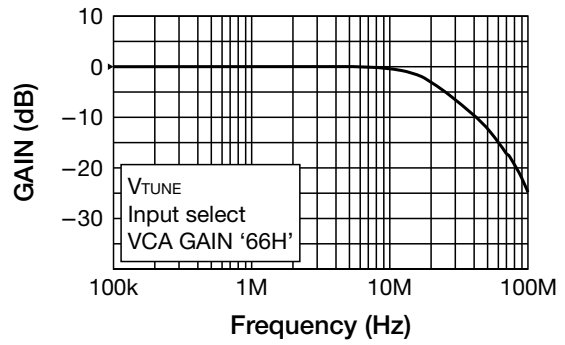


Frequency characteristic 2

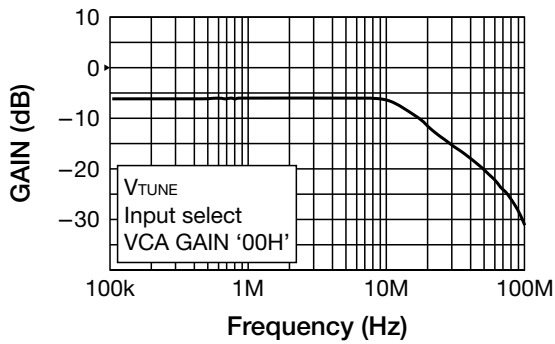
■ VTUNE—OUT1 THRU



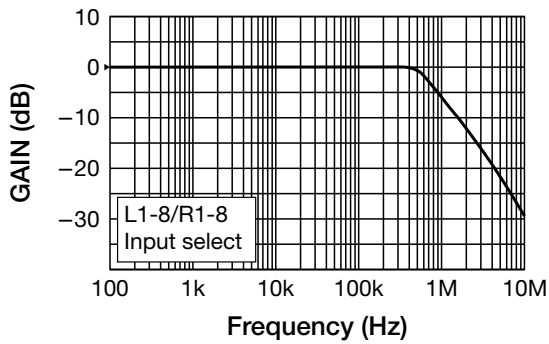
■ VTUNE—OUT1 THRU



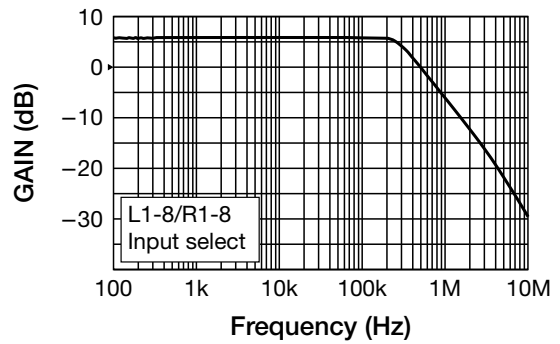
■ VTUNE—OUT1 THRU



■ AUDIO—OUT (0dB)

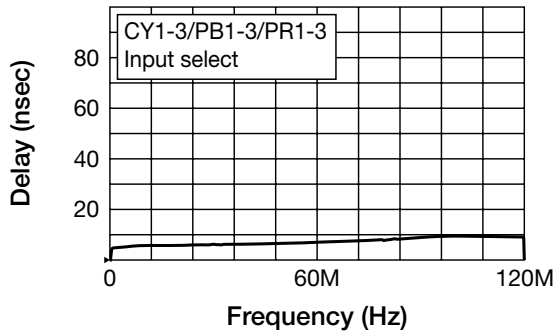


■ AUDIO—OUT (6dB)

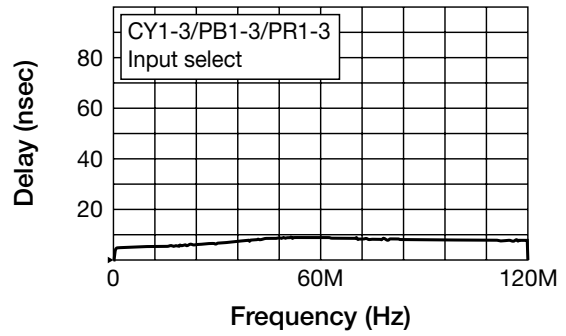


Group delay 1

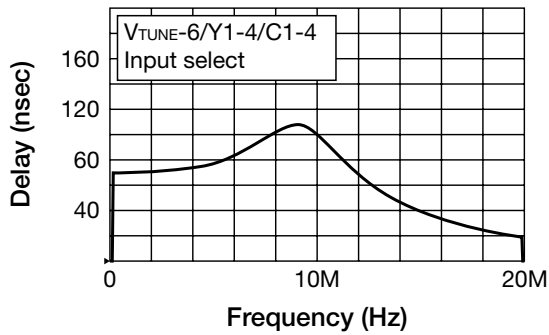
■ OUT1 THRU



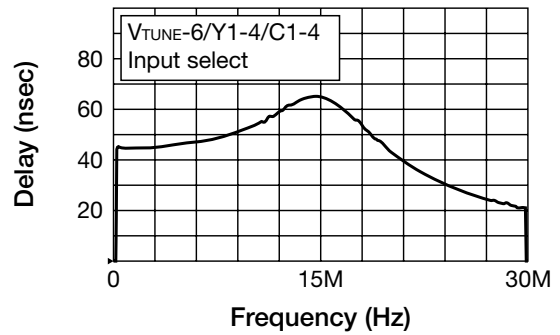
■ OUT2 THRU



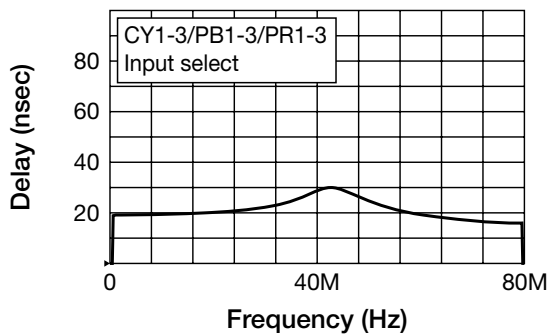
■ OUT1 LPF1 (fc=6.75MHz)



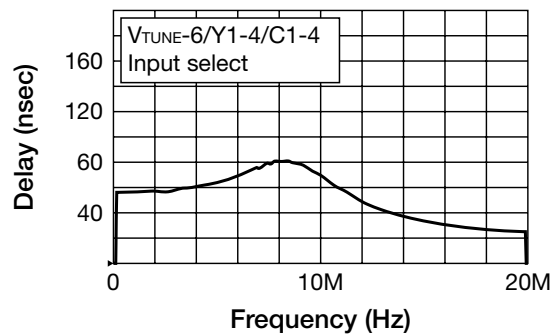
■ OUT1 LPF2 (fc=13.5MHz)



■ OUT1 LPF3 (fc=37.5MHz)

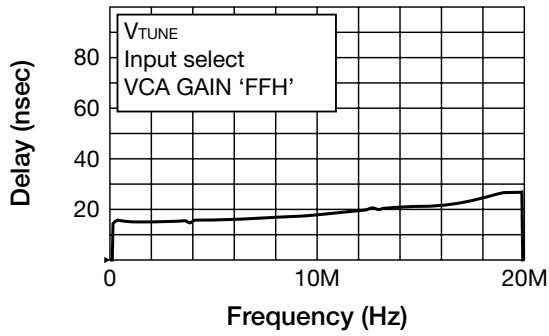


■ OUT3 (fc=6.75MHz)

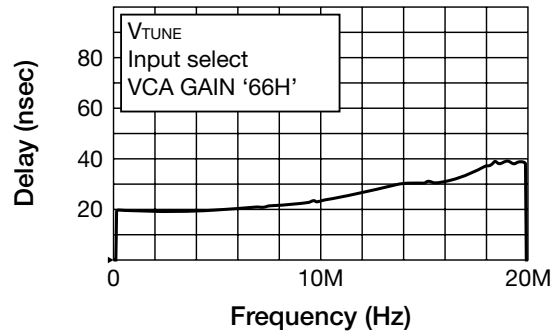


Group delay 2

■ VTUNE—OUT1 THRU



■ VTUNE—OUT1 THRU



■ VTUNE—OUT1 THRU

