

# 2-SCART Compatible AV Switch for DVD Recorders for Europe Monolithic IC MM1764

## Outline

This IC is a one-chip IC integrating an I<sup>2</sup>C BUS controlled AV switch with 6 inputs and 3 outputs with a 6-channel video driver with a built-in LPF. 2 outputs among 3 outputs of the AV switch are 75Ω drivers, which is ideal for analog interface for recording equipment such as 2-SCART compatible DVD recorders for Europe.

## Features

1. Serially controlled with I<sup>2</sup>C BUS
2. Provided in a small package (QFP-64: 0.8mm pitch) with an extensive function of a switch + driver
3. 6-channel video driver including a high performance 4th-order LPF
4. Audio output that is 0dB/6dB programmable and includes a newly-developed adjustable gain amplifier
5. Includes auto power saving function when V<sub>CC</sub>=12V is off (between V<sub>CC</sub>=5V, 12V)

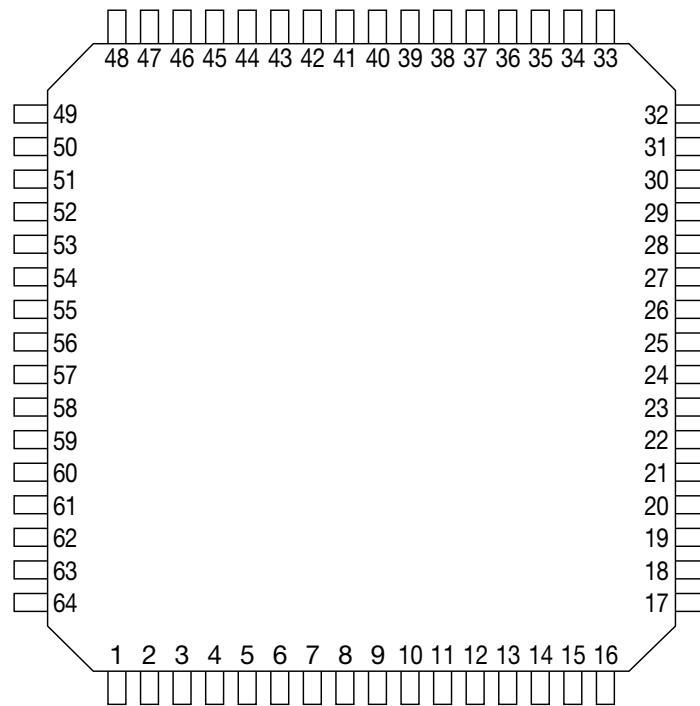
## Package

QFP-64E

## Applications

1. DVD recorder
2. VCR
3. STB
4. Recording equipment

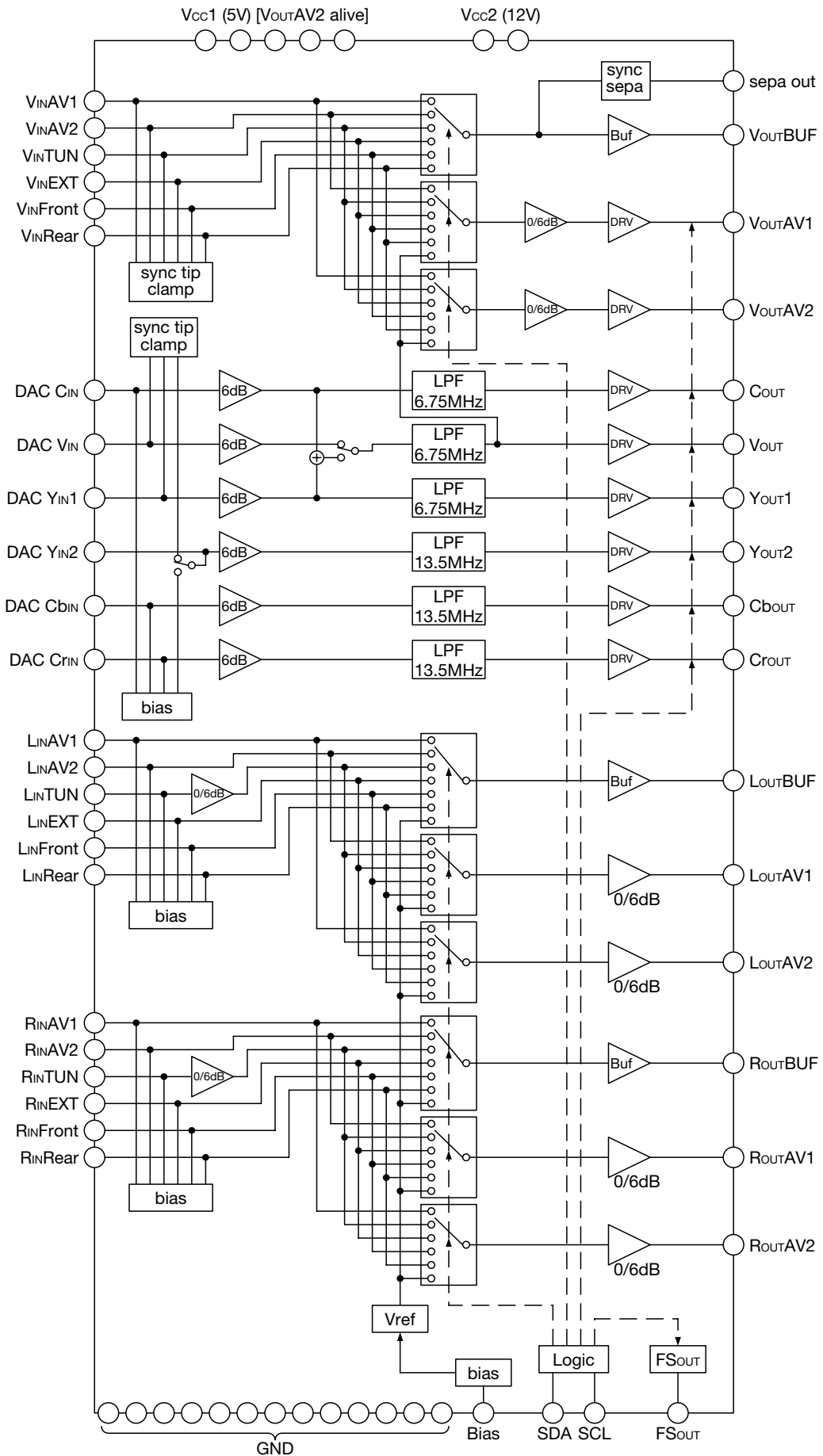
Pin Assignment



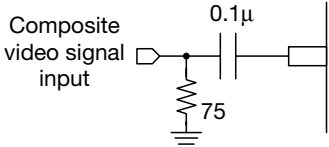
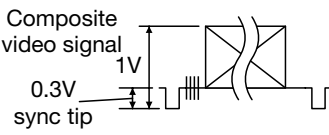
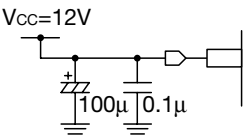
QFP-64E  
(TOP VIEW)

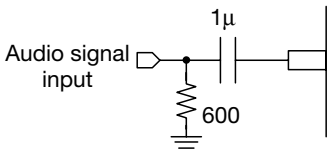
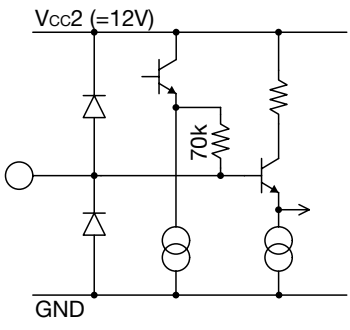
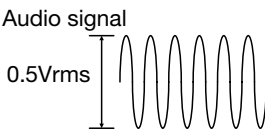
1	V <sub>IN</sub> Rear	17	BIAS	33	Y <sub>OUT</sub> 1	49	GND1
2	V <sub>CC</sub> 2 (12V)	18	DAC C <sub>IN</sub>	34	V <sub>OUT</sub>	50	V <sub>OUT</sub> AV2
3	L <sub>IN</sub> AV1	19	V <sub>CC</sub> 1 (5V)	35	C <sub>OUT</sub>	51	V <sub>OUT</sub> AV1
4	L <sub>IN</sub> AV2	20	DAC V <sub>IN</sub>	36	V <sub>CC</sub> 1 (5V)	52	V <sub>OUT</sub> BUF
5	L <sub>IN</sub> TUN	21	GND1	37	V <sub>CC</sub> 3 (5V)	53	V <sub>CC</sub> 1 (5V)
6	L <sub>IN</sub> EXT	22	DAC Y <sub>IN</sub> 1	38	SCL	54	sepa out
7	L <sub>IN</sub> Front	23	GND1	39	SDA	55	GND1
8	L <sub>IN</sub> Rear	24	DAC Y <sub>IN</sub> 2	40	GND3	56	V <sub>IN</sub> AV1
9	R <sub>IN</sub> AV1	25	GND1	41	GND2	57	V <sub>CC</sub> 1 (5V)
10	R <sub>IN</sub> AV2	26	DAC C <sub>BIN</sub>	42	R <sub>OUT</sub> AV2	58	V <sub>IN</sub> AV2
11	R <sub>IN</sub> TUN	27	GND1	43	R <sub>OUT</sub> AV1	59	GND1
12	R <sub>IN</sub> EXT	28	DAC C <sub>TIN</sub>	44	R <sub>OUT</sub> BUF	60	V <sub>IN</sub> TUN
13	R <sub>IN</sub> Front	29	GND1	45	L <sub>OUT</sub> AV2	61	GND1
14	R <sub>IN</sub> Rear	30	C <sub>ROUT</sub>	46	L <sub>OUT</sub> AV1	62	V <sub>IN</sub> EXT
15	GND2	31	C <sub>BOUT</sub>	47	L <sub>OUT</sub> BUF	63	GND1
16	FS <sub>OUT</sub>	32	Y <sub>OUT</sub> 2	48	V <sub>CC</sub> 2 (12V)	64	V <sub>IN</sub> Front

Block Diagram

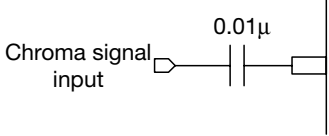
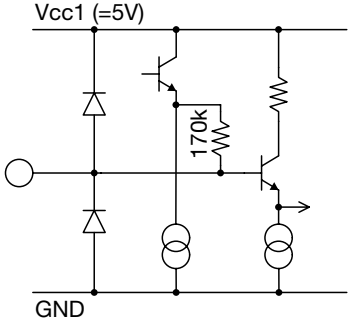
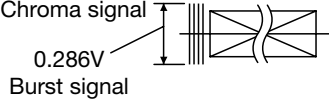
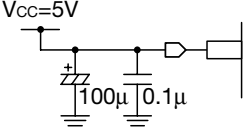


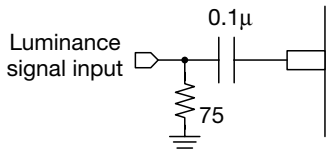
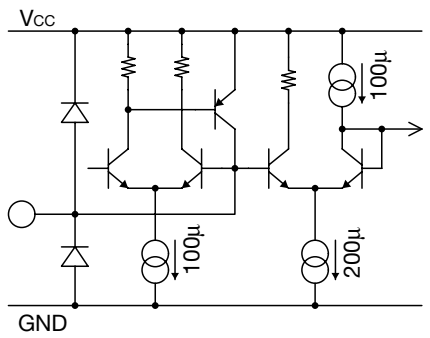
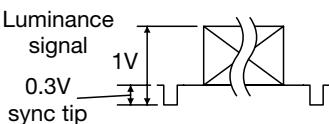
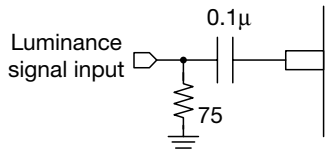
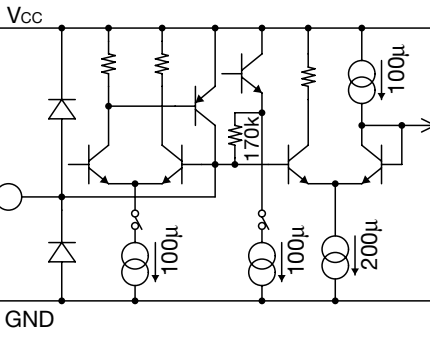
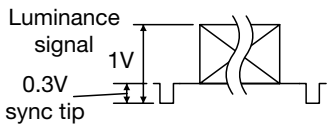
Pin Description

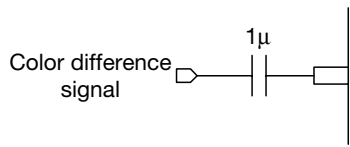
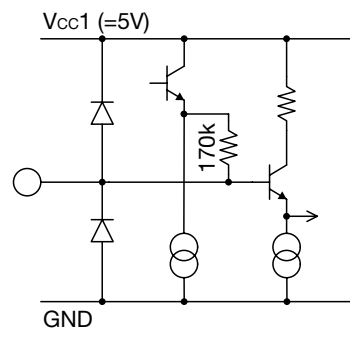
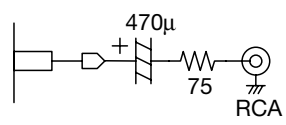
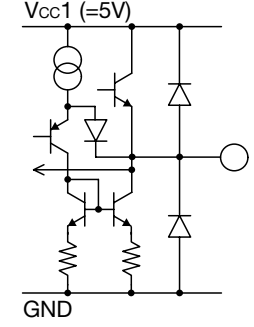
Pin No.	Pin name	Pin description	
1 20 56 58 60 62 64	V <sub>IN</sub> Rear DAC V <sub>IN</sub> V <sub>IN</sub> AV1 V <sub>IN</sub> AV2 V <sub>IN</sub> TUN V <sub>IN</sub> EXT V <sub>IN</sub> Front	<b>Function</b>	
		Composite signal input Input clamp Pin voltage: 1.1V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Composite video signal input</p> <p>0.1μ</p> <p>75</p> <p>When not using it: open</p>	
		<b>Input signal</b>	
 <p>Composite video signal</p> <p>1V</p> <p>0.3V sync tip</p>			
2 48	V <sub>CC</sub> 2	<b>Function</b>	
		Voltage supply It is a supply voltage impression terminal. Please impress 12V. Please arrange a bypass capacitor near the terminal.  V <sub>CC</sub> 2: Audio-V <sub>CC</sub>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>V<sub>CC</sub>=12V</p> <p>100μ 0.1μ</p>	
<b>Input signal</b>			
DC voltage: +11.2~+12.8V			

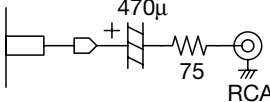
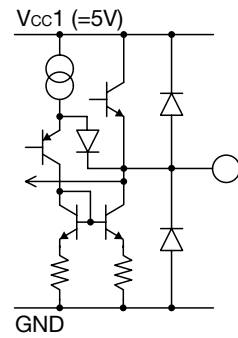
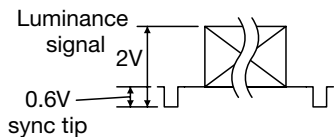
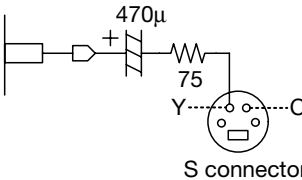
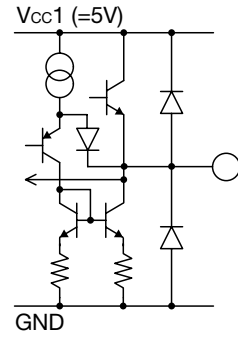
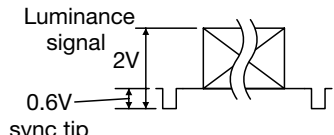
Pin No.	Pin name	Pin description	
		<b>Function</b>	
		Audio signal input Input impedance: 70k $\Omega$ typ. Pin voltage: 7.0V typ. Input dynamic range: 3Vrms min.	
3	L <sub>IN</sub> AV1		
4	L <sub>IN</sub> AV2		
5	L <sub>IN</sub> TUN		
6	L <sub>IN</sub> EXT		
7	L <sub>IN</sub> Front		
8	L <sub>IN</sub> Rear		
9	R <sub>IN</sub> AV1		
10	R <sub>IN</sub> AV2		
11	R <sub>IN</sub> TUN		
12	R <sub>IN</sub> EXT		
13	R <sub>IN</sub> Front		
14	R <sub>IN</sub> Rear		
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Input signal</b>	
			
15	GND2	<b>Function</b>	
21	GND1	Ground GND1: Video-GND, GND2: Audio-GND, GND3: Digital-GND	
23	GND1		
25	GND1		
27	GND1		
29	GND1		
40	GND3		
41	GND2		
49	GND1		
55	GND1		
59	GND1		
61	GND1		
63	GND1		
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<b>Input signal</b>	

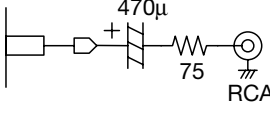
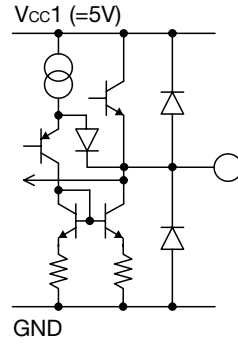
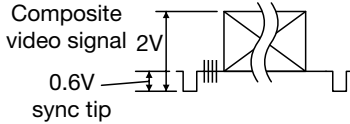
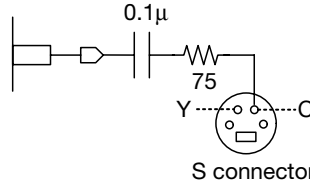
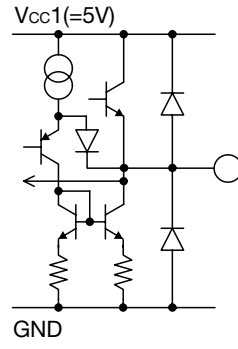
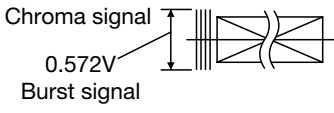
Pin No.	Pin name	Pin description																	
16	FS <sub>OUT</sub>	<b>Function</b>																	
		<p>DC output for SCART interface</p> <p>It is the terminal which outputs Function switch signal of SCART interface. The ternary output of L/M/H is controllable by I<sup>2</sup>C control. (refer to Switch Control Table)</p> <p>Output impedance: 500Ω typ.                      Low level output voltage: 0V typ.                      Middle level output voltage: 6V typ.                      High level output voltage: 10V typ.</p>																	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																
		<p>When not using it: open</p>																	
		<p style="text-align: center;"><b>Output signal</b></p> <p>DC voltage:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>b01</th> <th>b00</th> <th colspan="2">DC<sub>OUT</sub></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>L</td> <td>Level 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>M</td> <td>Level 1A</td> </tr> <tr> <td>1</td> <td>0</td> <td rowspan="2">H</td> <td rowspan="2">Level 1B</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </tbody> </table>		b01	b00	DC <sub>OUT</sub>		0	0	L	Level 0	0	1	M	Level 1A	1	0	H	Level 1B
b01	b00	DC <sub>OUT</sub>																	
0	0	L	Level 0																
0	1	M	Level 1A																
1	0	H	Level 1B																
1	1																		
17	BIAS	<b>Function</b>																	
		<p>BIAS</p> <p>All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.</p> <p>Input impedance: 8.6kΩ typ.</p>																	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																
		<p>When not using it: open</p>																	
		<p style="text-align: center;"><b>Output signal</b></p>																	

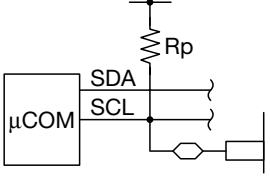
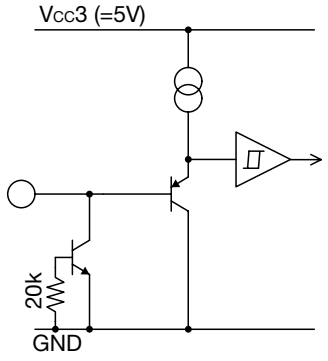
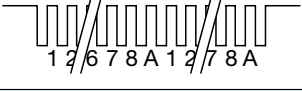
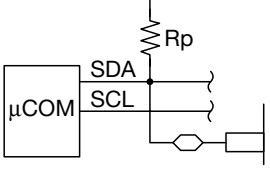
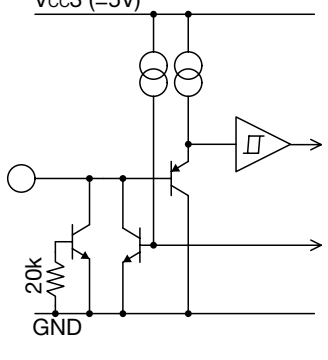
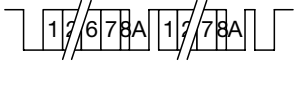
Pin No.	Pin name	Pin description	
18	DAC C <sub>IN</sub>	<b>Function</b>	
		Chroma signal input  Input bias Pin voltage: 2.4V typ. Input impedance: 170kΩ typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Chroma signal input</p> <p style="text-align: center;">0.01µ</p> <p style="text-align: center;">When not using it: open</p>	
		 <p>Vcc1 (=5V)</p> <p style="text-align: center;">170k</p> <p style="text-align: center;">GND</p>	
<b>Input signal</b>			
		 <p>Chroma signal</p> <p style="text-align: center;">0.286V</p> <p>Burst signal</p>	
19 36 37 53 57	Vcc1 Vcc1 Vcc3 Vcc1 Vcc1	<b>Function</b>	
		Voltage supply It is a supply voltage impression terminal. Please impress 5V. Please arrange a bypass capacitor near the terminal.  Vcc1: Video-Vcc, Vcc3: Digital-Vcc	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Vcc=5V</p> <p style="text-align: center;">100µ 0.1µ</p>	
		<b>Input signal</b>	
		DC voltage: +4.5~+5.5V	

Pin No.	Pin name	Pin description	
22	DAC Y <sub>IN1</sub>	<b>Function</b>	
		Luminance signal input Input clamp Pin voltage: 1.1V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Input signal</b>			
			
24	DAC Y <sub>IN2</sub>	<b>Function</b>	
		Luminance signal (G-signal) input Input clamp or bias select Pin voltage: 1.1V typ. (Clamp select) 2.4V typ. (Bias select) Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Input signal</b>			
			

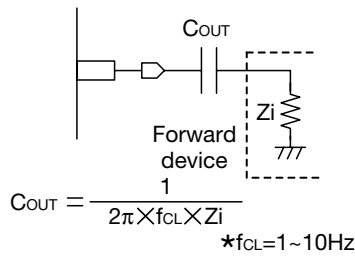
Pin No.	Pin name	Pin description	
26 28	DAC C <sub>bIN</sub> DAC C <sub>rIN</sub>	<b>Function</b>	
		Color difference signal input Input bias Pin voltage: 2.4V typ. Input impedance: 170kΩ typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Color difference signal</p> <p>1µ</p> <p>When not using it: open</p>	 <p>Vcc1 (=5V)</p> <p>170k</p> <p>GND</p>
		<b>Input signal</b>	
		Color difference signal 0.7V	
30 31	C <sub>rOUT</sub> C <sub>bOUT</sub>	<b>Function</b>	
		Color difference output It is a terminal for the Color difference signal external output.  Pin voltage: 2.4V typ. Load resistance: 150Ω × 2 Stray capacitance max.: 20pF	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>470µ</p> <p>75</p> <p>RCA</p> <p>When not using it: open</p>	 <p>Vcc1 (=5V)</p> <p>GND</p>
		<b>Output signal</b>	
		Color difference signal 1.4V	

Pin No.	Pin name	Pin description	
32	Yout2	<b>Function</b>	
		<p>Luminance output (525p) It is a terminal for a Luminance signal (525p) external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Output signal</b>			
			
33	Yout1	<b>Function</b>	
		<p>Luminance output (525i) It is a terminal for a Luminance signal (525i) external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Output signal</b>			
			

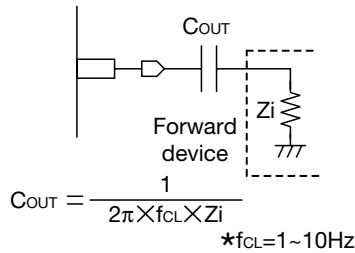
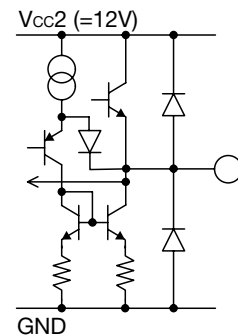
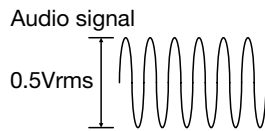
Pin No.	Pin name	Pin description	
34 50 51	V <sub>OUT</sub> V <sub>OUTAV2</sub> V <sub>OUTAV1</sub>	<b>Function</b>	
		<p>Composite video output It is a terminal for a composite video signal external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: 150Ω × 2 Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Output signal</b>			
<p>SDTV Composite video signal 2V 0.6V sync tip</p> 			
35	C <sub>OUT</sub>	<b>Function</b>	
		<p>Chroma output It is a terminal for the Chroma signal external output.</p> <p>Pin voltage: 2.4V typ. Load resistance: 150Ω × 2 Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
<b>Output signal</b>			
<p>Chroma signal 0.572V Burst signal</p> 			

Pin No.	Pin name	Pin description	
38	SCL	<b>Function</b>	
		Clock input of I <sup>2</sup> C BUS It is the terminal which connects the SCL line of I <sup>2</sup> C BUS.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  </div> <div style="text-align: center;">  </div> </div>	
<b>Input signal</b>			
Input signal Clock signal			
			
39	SDA	<b>Function</b>	
		DATA I/O of I <sup>2</sup> C BUS It is the terminal which connects the SDA line of I <sup>2</sup> C BUS.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  </div> <div style="text-align: center;">  </div> </div>	
<b>Input output signal</b>			
Input signal Control registers Output signal States registers			
			

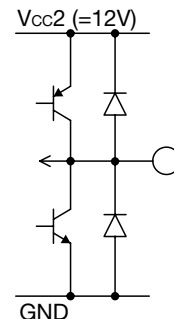
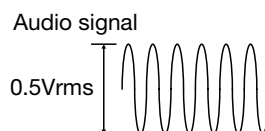
Pin No.	Pin name	Pin description
42 43 45 46	RoutAV2 RoutAV1 LoutAV2 LoutAV1	<b>Function</b>
		<p>Audio signal output It is a terminal for a audio signal external output.</p> <p>Pin voltage: 6.3V typ. Load resistance: 600Ω max. Stray capacitance max.: 20pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>
44 47	RoutBUF LoutBUF	<b>Function</b>
		<p>Audio signal output It is a terminal for a audio signal output.</p> <p>Pin voltage: 6.3V typ. Load resistance: 1kΩ max. Stray capacitance max.: 20pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>



When not using it: open



When not using it: open



Pin No.	Pin name	Pin description	
54	sepa out	<b>Function</b>	
		Composite sync output It is a terminal for a sync output of V <sub>OUT</sub> BUF (52pin) output signal.  Sync current: 3mA min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<b>Output signal</b>	
		Composite sync	

### Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-55~+150	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Supply voltage	V <sub>CC max.</sub>	13	V
Allowable loss	P <sub>d</sub>	700	mW

### Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
V <sub>CC1</sub> Operating voltage	V <sub>CC1OP</sub>	4.5~5.5	V
V <sub>CC2</sub> Operating voltage	V <sub>CC2OP</sub>	11.2~12.8	V

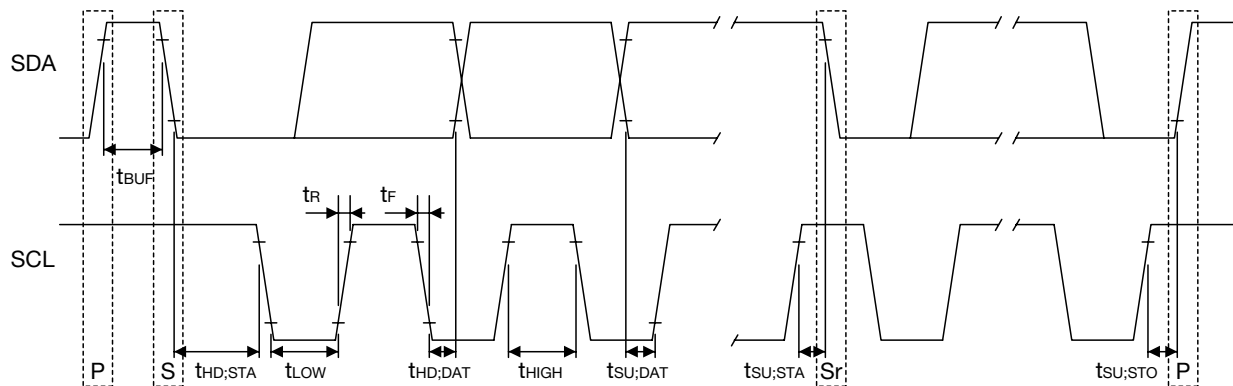
**Electrical Characteristics** (Except where noted otherwise Ta=25°C, VCC1=5V, VCC2=12V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
VCC (5V) supply current		ICC1	No signal	74	105	136	mA
VCC (12V) supply current		ICC2	No signal	19	27	35	mA
VCC (5V) supply current at standby		ICC3	No signal	21	29	37	mA
FS <sub>OUT</sub> Output voltage		H	RL=10kΩ	9.5	10.5	12	V
		M		4.5	6	7	V
		L		0	0.01	2	V
Terminal voltage	Video input (clamp)	V <sub>INCn</sub>		0.8	1.1	1.4	V
	Video input (bias)	V <sub>INBn</sub>		2.1	2.4	2.7	V
	Audio input	A <sub>INn</sub>		6.5	7.0	7.5	V
	Video output (clamp)	V <sub>OUTCn</sub>			1.1		V
	Video output (bias)	V <sub>OUTBn</sub>			2.4		V
	Audio output	A <sub>OUTn</sub>			6.3		V
[V <sub>OUTBUF</sub> ]							
Voltage gain		G <sub>Vn</sub>	SIN wave: 1V f=100kHz	-0.3	0	0.3	dB
Frequency characteristic		f <sub>Vn</sub>	SIN wave: 1V 10MHz/100kHz	-1	0	1	dB
Output dynamic range		DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.9		V
Differential gain		DG <sub>Vn</sub>	Staircase signal 1V		0.2	1	%
Differential phase		DP <sub>Vn</sub>	Staircase signal 1V		0.1	1	deg
[V <sub>OUTAV1</sub> , V <sub>OUTAV2</sub> ]							
Voltage gain		G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic		f <sub>Vn</sub>	SIN wave: 1V 7MHz/100kHz	-1	0	1	dB
Output dynamic range		DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG <sub>Vn</sub>	Staircase signal 1V		2	3	%
Differential phase		DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg
[C <sub>OUT</sub> , V <sub>OUT</sub> , Y <sub>OUT1</sub> ]							
Voltage gain		G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1		f <sub>1Vn</sub>	SIN wave: 1V 6.75MHz/100kHz	-1	0	1	dB
Frequency characteristic 2		f <sub>2Vn</sub>	SIN wave: 1V 27MHz/100kHz		-30	-24	dB
Output dynamic range		DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG <sub>Vn</sub>	Staircase signal 1V		1	2	%
Differential phase		DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg
Signal/Noise		SN <sub>Vn</sub>	BW: 100kHz~6MHz		80		dB
Group delay		t <sub>Vn</sub>	at 100kHz		50	80	ns
Group delay deviation		Δt <sub>Vn</sub>	to 3.58MHz		5	10	ns
			to 4.43MHz		10	20	ns
			to 6MHz		20	28	ns

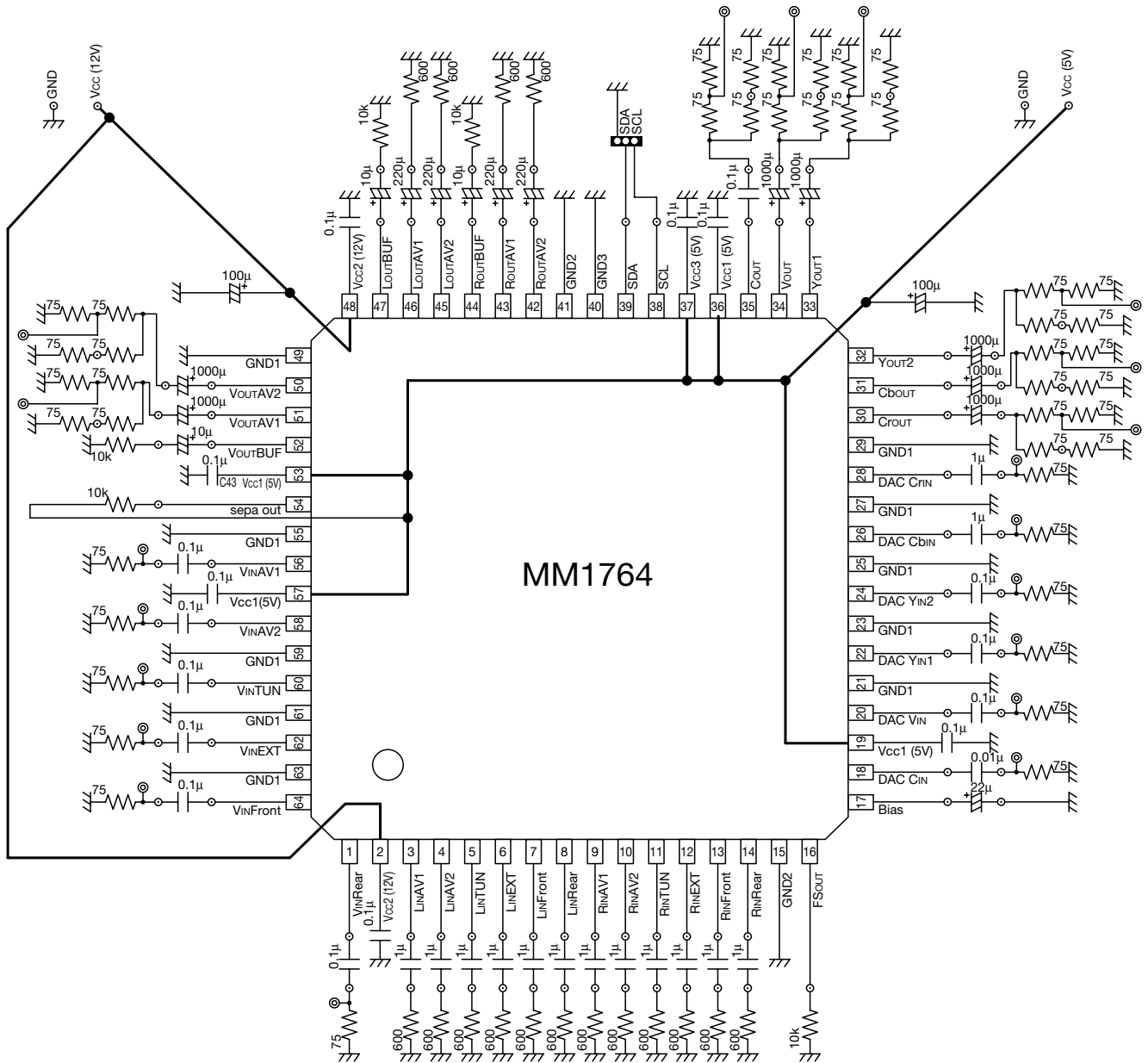
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
<b>[Y<sub>OUT2</sub>, C<sub>bOUT</sub>, C<sub>rOUT</sub>]</b>						
Voltage gain	G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	f <sub>1V (YOUT2)</sub>	100 [IRE] SIN wave + 40 [IRE] sync 13.5MHz/100kHz	-1	0	1	dB
Frequency characteristic 2	f <sub>2V (CbOUT, CrOUT)</sub>	100 [IRE] SIN wave + 40 [IRE] sync 6.75MHz/100kHz	-1	0	1	dB
Frequency characteristic 3	f <sub>3Vn</sub>	100 [IRE] SIN wave + 40 [IRE] sync 54MHz/100kHz		-30	-24	dB
Output dynamic range	DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG <sub>Vn</sub>	Staircase signal 1V		1	2	%
Differential phase	DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg
Signal/Noise	SN <sub>Vn</sub>	BW: 100kHz~6MHz		80		dB
Group delay	t <sub>Vn</sub>	at 100kHz		25	50	ns
Group delay deviation	Δt <sub>1V (YOUT2)</sub>	to 2MHz		1	10	ns
		to 8MHz		2	10	ns
		to 12MHz		10	20	ns
Group delay deviation	Δt <sub>2V (CbOUT)</sub> Δt <sub>2V (CrOUT)</sub>	to 1MHz		1	10	ns
		to 4MHz		2	10	ns
		to 6MHz		10	20	ns
<b>[L<sub>OUTBUF</sub>, R<sub>OUTBUF</sub>]</b>						
Voltage gain	G <sub>0An</sub>	SIN wave: 1Vrms f=1kHz	-0.5	0	0.5	dB
	G <sub>6An</sub>	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
Output dynamic range	DR <sub>An</sub>	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion	THD <sub>An</sub>	SIN wave: 1kHz V <sub>OUT</sub> =1Vrms		0.005	0.05	%
Output noise voltage	VN <sub>An</sub>	A curve		3.0		μVrms
Output offset voltage	VOF <sub>An</sub>	at the switching		0	±15	mV
<b>[L<sub>OUTAV1</sub>, L<sub>OUTAV2</sub>, R<sub>OUTAV1</sub>, R<sub>OUTAV2</sub>]</b>						
Voltage gain	G <sub>0An</sub>	SIN wave: 1Vrms f=1kHz	-0.5	0	0.5	dB
	G <sub>6An</sub>	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
	G <sub>12An</sub>	SIN wave: 0.25Vrms f=1kHz	11.5	12	12.5	dB
Output dynamic range	DR <sub>An</sub>	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion	THD <sub>An</sub>	SIN wave: 1kHz V <sub>OUT</sub> =1Vrms		0.005	0.05	%
Output noise voltage	VN <sub>An</sub>	A curve		5		μVrms
Output offset voltage	VOF <sub>An</sub>	at the switching		0	±15	mV

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Crosstalk	V <sub>OUT</sub>	CT <sub>Vn</sub>			-60	-50	dB
	L <sub>OUT</sub> , R <sub>OUT</sub>	CT <sub>An</sub>			-90	-70	dB
Video input impedance		Z <sub>inVn</sub>	18, (24), 26, 28 pin	120	170	220	kΩ
Audio input impedance		Z <sub>inAn</sub>	L: 3~8 pin, R: 9~14 pin	50	70	90	kΩ
Output impedance		Z <sub>OUT</sub>	FS <sub>OUT</sub>	300	500	800	Ω
Standby V <sub>CC2</sub> input voltage	L	V <sub>THVCC2L</sub>				2.0	V
	H	V <sub>THVCC2H</sub>		3.5			V
[Sync out]							
Sync sepa level		V <sub>SEPA</sub>		15	30	60	mV
Sync sepa output voltage	L	V <sub>SOL</sub>	2mA sync			0.4	V
	H	V <sub>SOH</sub>	10kΩ pull-up	4.8			V
[I <sup>2</sup> C condition]							
Input voltage L		V <sub>IL</sub>		0		0.7	V
Input voltage H		V <sub>IH</sub>		2.1		5.0	V
SDA low level output voltage		V <sub>OL</sub>	SDA sink 3mA	0		0.4	V
High level input current		I <sub>IH</sub>	SDA, SCL=4.5V	-10		10	μA
Low level input current		I <sub>IL</sub>	SDA, SCL=0.4V	-10		10	μA
Clock frequency		f <sub>SCL</sub>				100	kHz
Data transfer wait time		t <sub>BUF</sub>		4.7			μs
SCL start hold time		t <sub>HD;STA</sub>		4.0			μs
SCL low level hold time		t <sub>LOW</sub>		4.7			μs
SCL high level hold time		t <sub>HIGH</sub>		4.0			μs
Start condition setup time		t <sub>SU;STA</sub>		4.7			μs
SDA data hold time		t <sub>HD;DAT</sub>		0			μs
SDA data setup time		t <sub>SU;DAT</sub>		250			ns
SDA, SCL rise time		t <sub>R</sub>				1000	ns
SDA, SCL fall time		t <sub>F</sub>				300	ns
Stop condition setup time		t <sub>SU;STO</sub>		4.0			μs

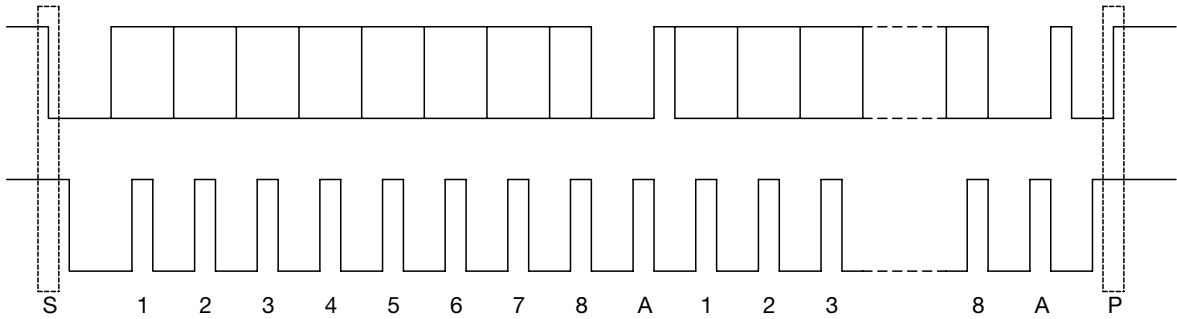
Note: I<sup>2</sup>C condition



Measuring Circuit



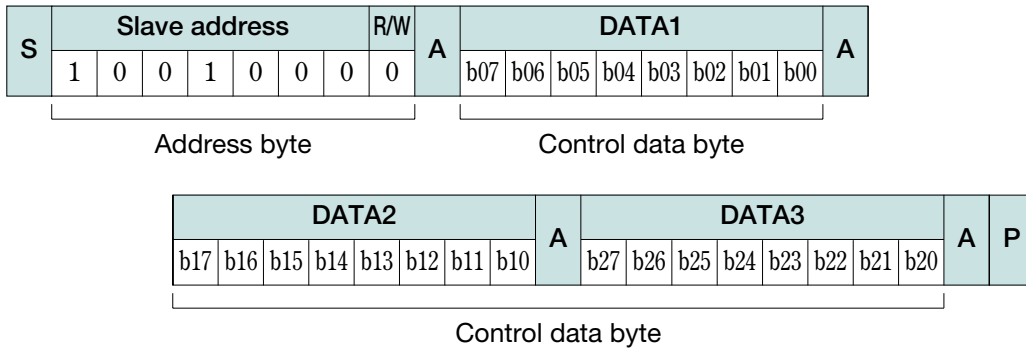
I<sup>2</sup>C BUS



I<sup>2</sup>C BUS is inter IC bus system controlled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used as control register. MM1764 slave address is 90H. The next page figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

[Control data]

No.	Control DATA condition							
	b07	b06	b05	b04	b03	b02	b01	b00
DATA1	V <sub>OUT</sub> BUF select			V <sub>OUT</sub> AV1 select			FS CTRL	
DATA2	b17	b16	b15	b14	b13	b12	b11	b10
	V <sub>OUT</sub> AV2 select			L/R <sub>OUT</sub> BUF select			L/R <sub>AV1</sub> gain	L/R <sub>AV2</sub> gain
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	L/R <sub>OUT</sub> AV1 select			L/R <sub>OUT</sub> AV2 select			mix select	clamp bias sel

MM1764 consists of one address byte and three control data bytes (4bytes in total). All data over the limited length (5th and subsequent bytes) are fully neglected. For details of the control contents of switches, refer to the separate table.

■ Switch Control Table

■ Control register 1 (2nd byte)

Control register 1								V <sub>OUT</sub> BUF select	V <sub>OUT</sub> AV1 select	FS CTRL
b07	b06	b05	b04	b03	b02	b01	b00			
0	0	0						V <sub>INTUN</sub>		
0	0	1						V <sub>INAV1</sub>		
0	1	0						V <sub>INAV2</sub>		
0	1	1						V <sub>INEXT</sub>		
1	0	0						V <sub>IN</sub> Front		
1	0	1								
1	1	0								
1	1	1						V <sub>IN</sub> Rear		
			0	0	0				V <sub>INAV2</sub>	
			0	0	1				V <sub>INTUN</sub>	
			0	1	0				V <sub>INEXT</sub>	
			0	1	1				DAC V <sub>IN</sub>	
			1	0	0			V <sub>IN</sub> Front		
			1	0	1					
			1	1	0					
			1	1	1			V <sub>IN</sub> Rear		
						0	0			Low
						0	1			Middle
						1	0			High
						1	1			

■ Control register 2 (3rd byte)

Control register 2								V <sub>OUT</sub> AV2 select	L/R <sub>OUT</sub> BUF select	L/R AV1 gain	L/R AV2 gain
b17	b16	b15	b14	b13	b12	b11	b10				
0	0	0						V <sub>INAV1</sub>			
0	0	1						V <sub>INTUN</sub>			
0	1	0						V <sub>INEXT</sub>			
0	1	1						DAC V <sub>IN</sub>			
1	0	0						V <sub>IN</sub> Front			
1	0	1									
1	1	0									
1	1	1						V <sub>IN</sub> Rear			
			0	0	0				mute		
			0	0	1				L/R <sub>INTUN</sub> (0dB)		
			0	1	0				L/R <sub>INTUN</sub> (6dB)		
			0	1	1				L/R <sub>INAV1</sub>		
			1	0	0				L/R <sub>INAV2</sub>		
			1	0	1				L/R <sub>INEXT</sub>		
			1	1	0				L/R <sub>IN</sub> Front		
			1	1	1				L/R <sub>IN</sub> Rear		
						0				0 dB	
						1				6 dB	
							0				0 dB
							1				6 dB

■ Control register 3 (4th byte)

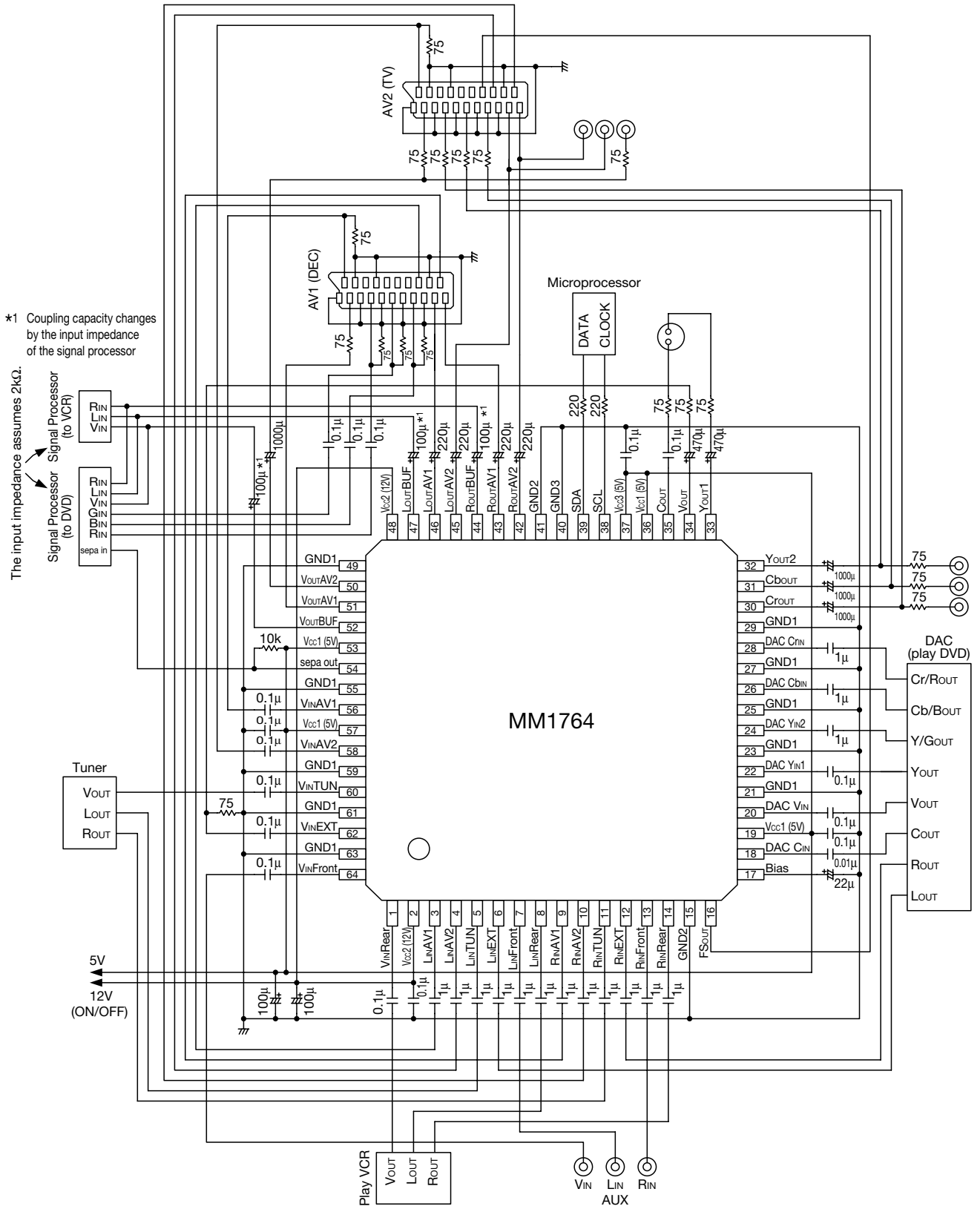
Control register 2								L/R <sub>OUT</sub> AV1	L/R <sub>OUT</sub> AV2	MIX	bias/clamp
b27	b26	b25	b24	b23	b22	b21	b20	select	select	select	select
0	0	0						mute			
0	0	1						L/R <sub>IN</sub> TUN (0dB)			
0	1	0						L/R <sub>IN</sub> TUN (6dB)			
0	1	1						L/R <sub>IN</sub> AV2			
1	0	0						L/R <sub>IN</sub> EXT			
1	0	1						L/R <sub>IN</sub> Front			
1	1	0						L/R <sub>IN</sub> Rear			
1	1	1									
			0	0	0				mute		
			0	0	1				L/R <sub>IN</sub> TUN (0dB)		
			0	1	0				L/R <sub>IN</sub> TUN (6dB)		
			0	1	1				L/R <sub>IN</sub> AV1		
			1	0	0				L/R <sub>IN</sub> EXT		
			1	0	1				L/R <sub>IN</sub> Front		
			1	1	0				L/R <sub>IN</sub> Rear		
			1	1	1						
						0				V <sub>IN</sub>	
						1				Y/Cmix	
							0				bias
							1				clamp

[Status registers]

There is no preparation of the status register in MM1764. A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.

Application Circuit



\*1 Coupling capacity changes by the input impedance of the signal processor

The input impedance assumes 2kΩ.

Signal Processor (to VCR)

Signal Processor (to DVD)

Tuner

5V  
12V (ON/OFF)

Play VCR

MM1764

Microprocessor

DAC (play DVD)