

# HD-Compatible Video Driver IC Monolithic IC MM1757 Series

April 28, 2009

## Outline

This IC is a two-channel 75Ω video driver IC supporting HD (720p/D4, 1080i/D3). It provides the input and output for composite video (V), S-Video (Y, C), and Y color difference (CY, Cb, Cr) (only Y color difference input/output is HD-compatible). It supports both single and dual power supplies. If a single power supply is used, a sag correction circuit can reduce output capacitance, while no output capacitance is required if a dual power supply is used. It also includes an LPF (VCVS Butterworth) required after D/A conversion, D-terminal identification signal (line 1 - line 3) and S-terminal identification signal (S1, S2) output functions, which is ideal as an output driver for Hi-Vision (HD) signal output equipment such as set-top boxes (STBs) and DVD, Blu-ray recorders.

## Features

1. Supports the Hi-Vision signal
2. Supports single power supplies and dual power supplies
3. Includes a VCVS Butterworth LPF
4. Includes D-terminal identification signal (line 1 - line 3) and S-terminal identification signal (S1, S2) output functions (F rank)
5. Two types of IC control methods are available; I<sup>2</sup>C bus control and DC control with a control pin (F rank)

Item	Model	MM1757DH	MM1757EH	MM1757FH
Input/Output terminal		CY/Cb/Cr, CVBS, Y/C		
Power supply		Dual/Single	Single	Dual/Single
Output coupling capacitor		○/×	×	○/×
D Terminal		×	×	○
HD/SD switch		○	○	○
I <sup>2</sup> C Bus control		×	×	○
Clamp/Bias switch		×	○	○
CVBS/Y/C (Bus bandwidth/Stop Bus bandwidth)		6.75MHz/27MHz		
CY/Cb/Cr-SD (Bus bandwidth/Stop Bus bandwidth)		13.5MHz/54MHz		
CY/Cb/Cr-HD (Bus bandwidth/Stop Bus bandwidth)		37MHz/148MHz	30MHz/74MHz	30MHz/74MHz
Packages		HSOP-28	HSOP-28	HSOP-36

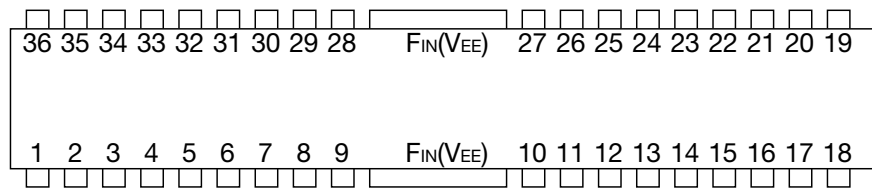
## Packages

1. HSOP-28 (D, E rank)
2. HSOP-36 (F rank)

## Applications

1. STB
2. DVD, Blu-ray Recorder

**Pin Assignment**

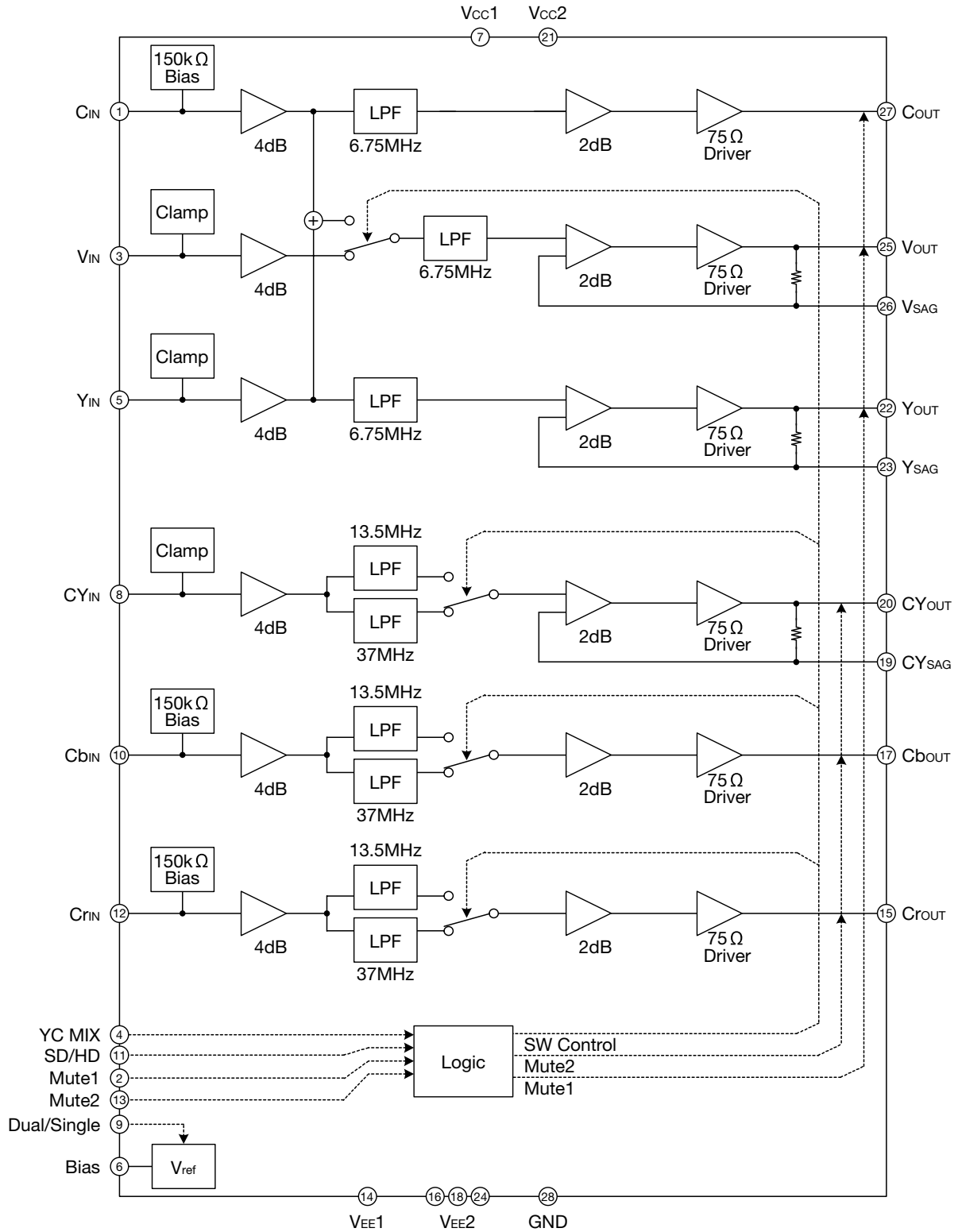


HSOP-36A  
(TOP VIEW)

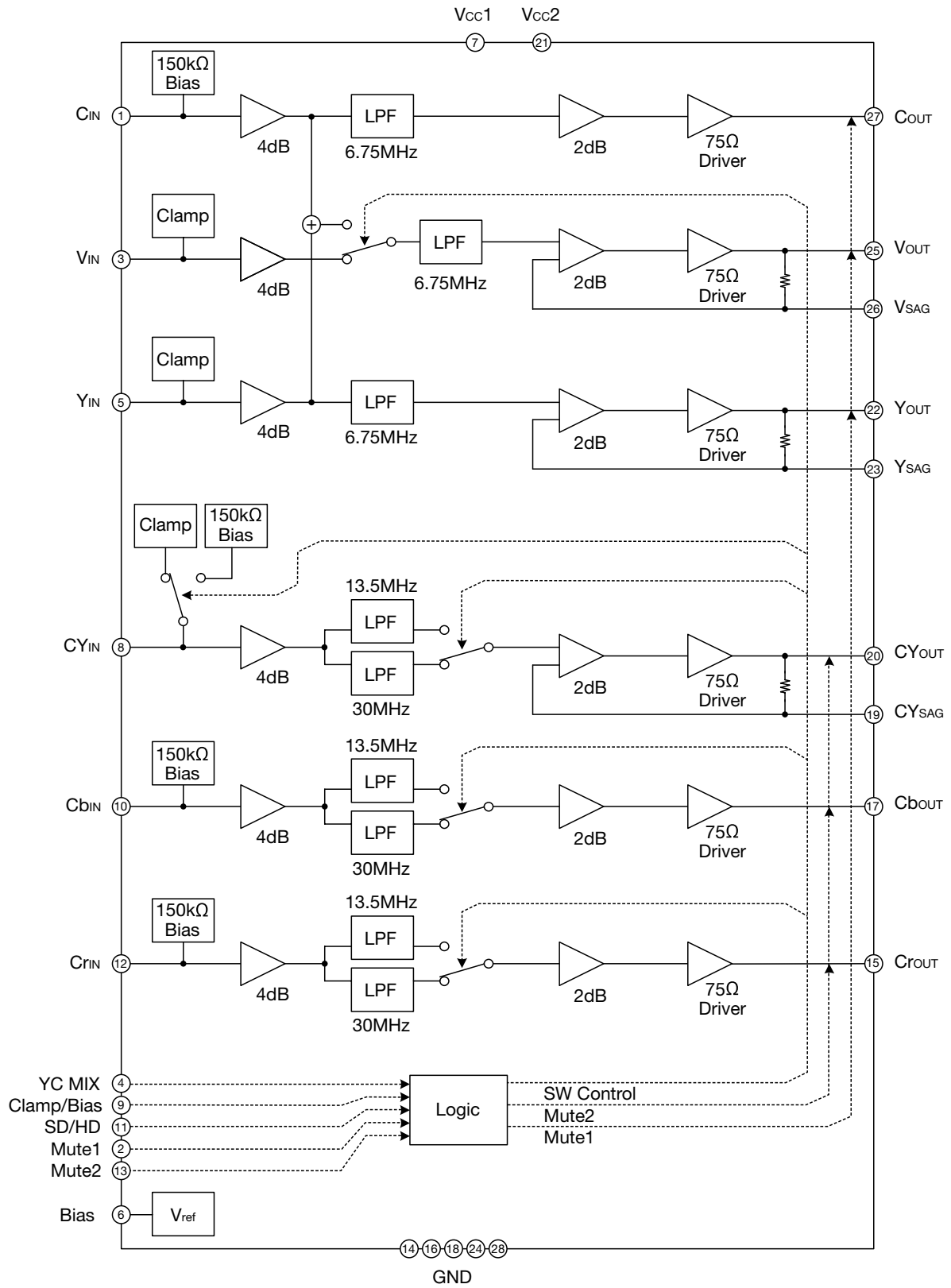
1	C <sub>IN</sub>	11	V <sub>CC1</sub>	21	V <sub>EE2</sub>	31	V <sub>EE2</sub>
2	Mute1	12	C <sub>YIN</sub>	22	C <sub>bOUT</sub>	32	V <sub>OUT</sub>
3	V <sub>IN</sub>	13	Clamp/Bias	23	Line2 out	33	V <sub>SAG</sub>
4	YC MIX	14	C <sub>bIN</sub>	24	V <sub>EE2</sub>	34	C <sub>OUT</sub>
5	Y <sub>IN</sub>	15	SD/HD	25	C <sub>YSAG</sub>	35	S1/S2 out
6	Dual/Single	16	C <sub>rIN</sub>	26	C <sub>YOUT</sub>	36	GND
7	Bias	17	Mute2	27	Line1 out		
8	SCL	18	V <sub>EE1</sub>	28	V <sub>CC2</sub>		
9	SDA	19	C <sub>rOUT</sub>	29	Y <sub>OUT</sub>		
10	Address	20	Line3 out	30	Y <sub>SAG</sub>		

Block Diagram

D rank

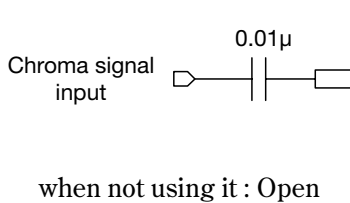
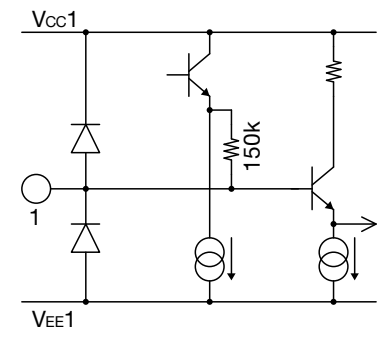
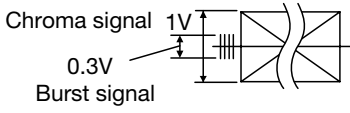
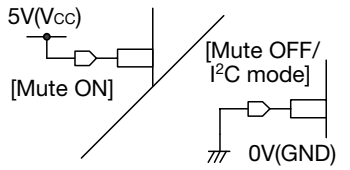
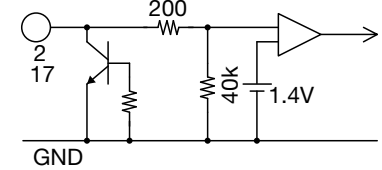


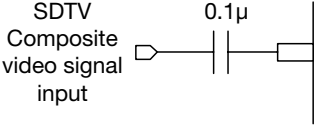
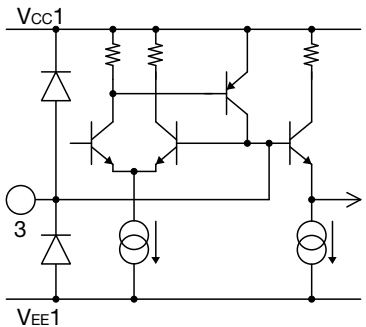
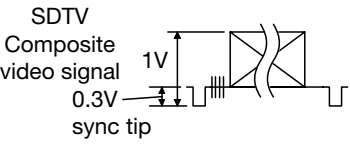
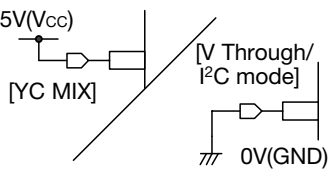
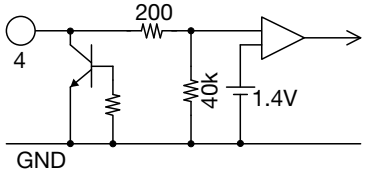
E rank

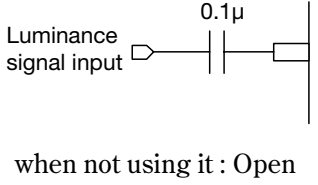
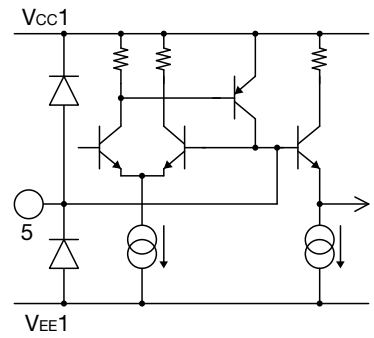
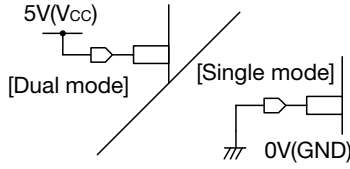
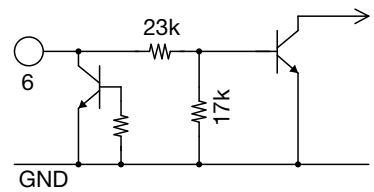


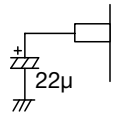
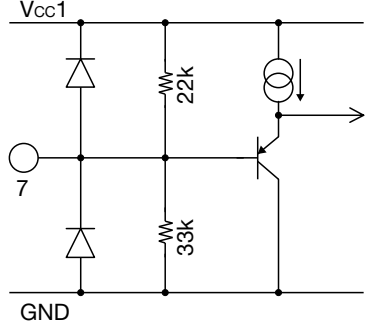
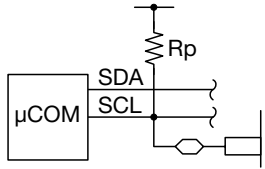
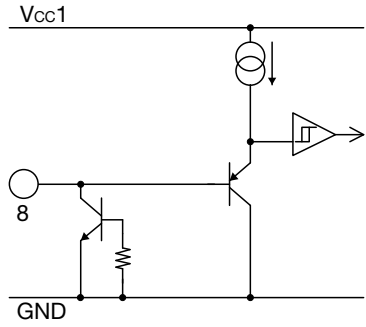



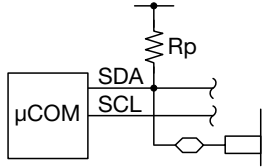
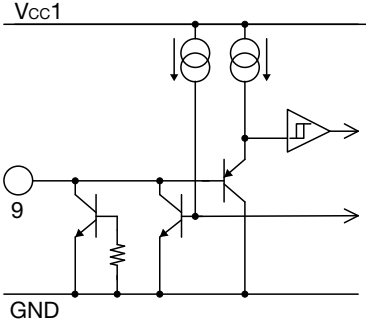
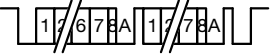
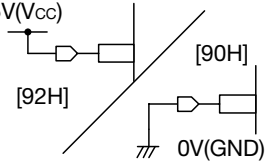
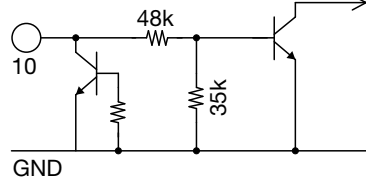
**Pin Description** (F rank)

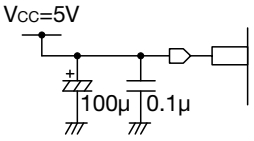
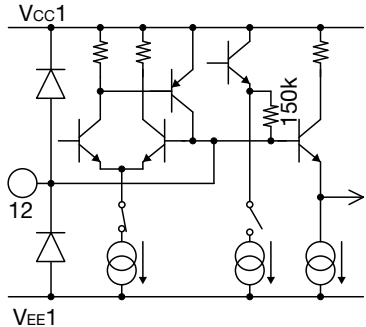
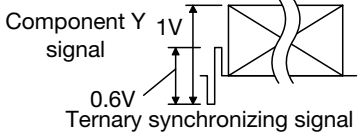
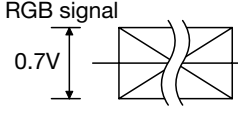
Pin No.	Pin name	Pin description	
1	C <sub>IN</sub>	<b>Function</b>	
		<p>Chroma Signal Input Pin to input chrominance signals of S-video. Bias input pin.</p> <p>Pin voltage: 2.5V typ. [at Single mode] Input impedance: 150kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Chroma signal input</p> <p>0.01µ</p> <p>when not using it : Open</p>	 <p>Vcc1</p> <p>1</p> <p>VEE1</p> <p>150k</p>
<b>Input signal</b>			
		 <p>Chroma signal 1V</p> <p>0.3V Burst signal</p>	
2 17	Mute1 Mute2	<b>Function</b>	
		<p>Mute select Select mute ON/OFF with a voltage applied to this pin. Mute1 controls C/V/Y. Mute2 controls CY/Cb/Cr.</p> <p>To select mute ON/OFF, I<sup>2</sup>C BUS can be also used. * See section Switch Control Table.</p> <p>Threshold : 1.4V typ. Input impedance : 40kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>5V(Vcc)</p> <p>[Mute ON]</p> <p>[Mute OFF/ I<sup>2</sup>C mode]</p> <p>0V(GND)</p> <p>when not using it : Open</p>	 <p>200</p> <p>40k</p> <p>1.4V</p> <p>GND</p>
<b>Input signal</b>			
		<p>DC Voltage : 0V(GND) to 5V(Vcc)</p>	

Pin No.	Pin name	Pin description	
3	V <sub>IN</sub>	<b>Function</b>	
		Composite Video Signal Input Pin to input composite video signals. Clamp input pin.  Pin voltage : 1.4V typ. [at Single mode]	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>SDTV Composite video signal input</p> <p>0.1µ</p> <p>when not using it : Open</p>	
		<b>Input signal</b>	
 <p>SDTV Composite video signal</p> <p>1V</p> <p>0.3V sync tip</p>			
4	YC MIX	<b>Function</b>	
		YC MIX select Select MIX mode/V through mode with a voltage applied to this pin.  To select YC MIX, I <sup>2</sup> C BUS can be also used. * See section Switch Control Table.  Threshold : 1.4V typ. Input impedance : 40kΩ typ.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>5V(V<sub>cc</sub>)</p> <p>[YC MIX]</p> <p>[V Through/ I<sup>2</sup>C mode]</p> <p>0V(GND)</p> <p>when not using it : Open</p>	
		<b>Input signal</b>	
DC Voltage : 0V(GND) to 5V(V <sub>cc</sub> )			

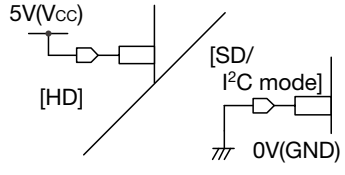
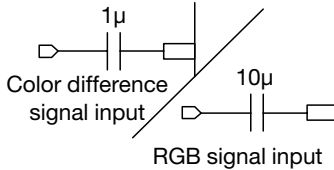
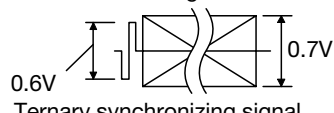
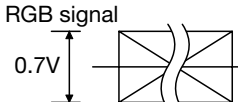
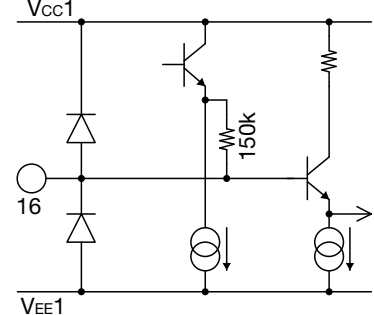
Pin No.	Pin name	Pin description	
5	Y <sub>IN</sub>	<b>Function</b>	
		Luminance Signal Input Pin to input luminance signals of S-video. Clamp input pin.  Pin voltage : 1.4V typ. [at Single mode]	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>	
6	Dual/Single	<b>Function</b>	
		Dual/Single Power Supply select Select (a) type of (a) power supply (single supply/dual power supplies) with a voltage applied to this pin. Single mode : V <sub>CC</sub> = 5V typ. , V <sub>EE</sub> = GND Dual mode : V <sub>CC</sub> = 5V typ. , V <sub>EE</sub> = -3V typ.  * See section Switch Control Table.  Threshold : 1.7V typ. Input impedance : 40kΩ typ.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>	
		DC Voltage : 0V(GND) to 5V(Vcc)	

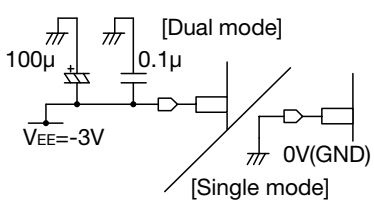
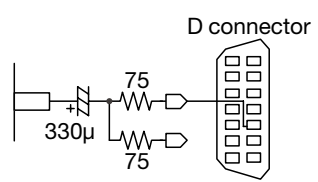
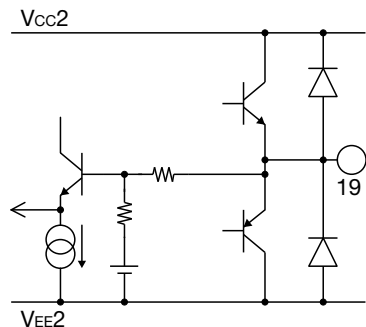

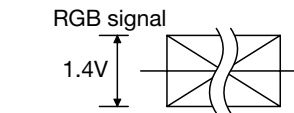
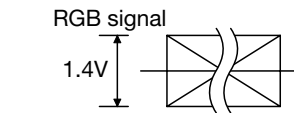
Pin No.	Pin name	Pin description	
7	Bias	<b>Function</b>	
		<p><b>Bias</b>                      All the reference voltages used inside the IC are produced according to the resistance divider of this pin.                      Pin to stabilize reference voltages, and reduce both power supply ripple and cross talk by decreasing impedance with an external 22<math>\mu</math>F.                       Input Impedance : 13k<math>\Omega</math> typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
<b>Input signal</b>			
		<b>Function</b>	
8	SCL	<p><b>Clock Input of I<sup>2</sup>C BUS</b>                      Pin to control the IC with I<sup>2</sup>C BUS along with SDA (9pin)                      Address (10pin) is used to select an address.                       * See section I<sup>2</sup>C BUS.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<b>Input signal</b>	
		<b>Input signal</b>	
		<p>Clock signal</p> 	

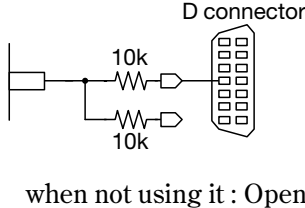
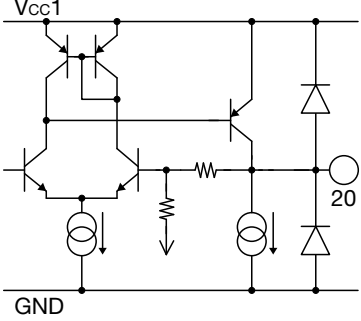
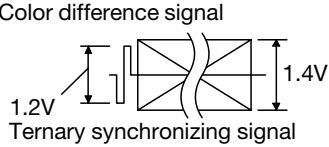
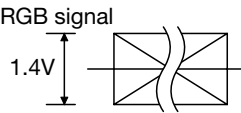
Pin No.	Pin name	Pin description	
9	SDA	<b>Function</b>	
		<p>DATA Input of I<sup>2</sup>C BUS                      Pin to control the IC with I<sup>2</sup>C BUS along with SCL (8pin).                      The Address pin (10pin) is used to select an address.</p> <p>★ See section I<sup>2</sup>C BUS.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<b>Input signal</b>	
<p>Controll registers</p> 			
10	Address	<b>Function</b>	
		<p>Slave Address select                      Select an I<sup>2</sup>C slave address 90H/92H with a voltage applied to this pin.</p> <p>★ See section I<sup>2</sup>C BUS.</p> <p>Threshold : 1.7V typ.                      Input impedance : 83kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<b>Input signal</b>	
<p>DC Voltage : 0V(GND) to 5V(Vcc)</p>			

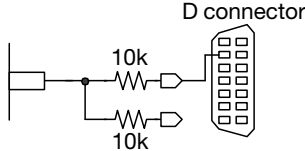
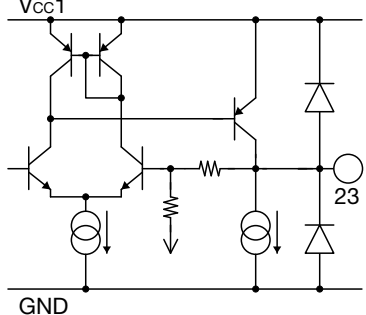
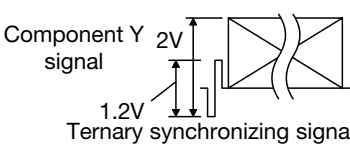
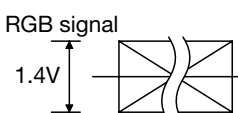
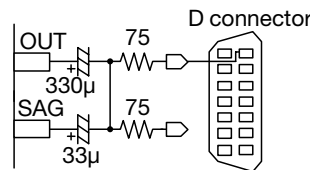
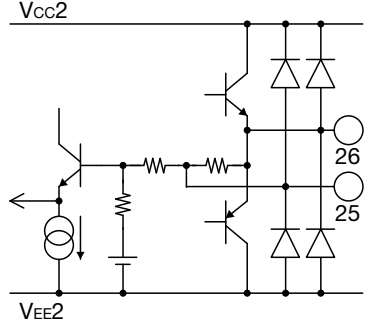
Pin No.	Pin name	Pin description
11 28	Vcc1 Vcc2	<b>Function</b>
		<p><b>Positive Voltage Supply</b>                      Pin to apply a positive supply voltage. Apply 5V.                      11pin and 28pin are not shorted inside the IC.                      Vcc2 is connected to an output stage circuit, and Vcc1 is connected to a circuit other than an output stage circuit.</p> <p>Note : Please be sure to short-circuit Vcc1 and Vcc2 externally.                      Note : When using dual power supplies, after VEE1 and VEE2 or simultaneously, turn on Vcc1 and Vcc2.                      Note : Please arrange power supply bypass capacitor near the terminal.</p>
		<b>External circuit</b>
		<b>Input signal</b>
		<b>Equivalent circuit diagram</b>
		
		<p>DC Voltage :                      4.5V~5.5V [at Single mode]                      4.7V~5.3V [at Dual mode]</p>
12	CY <sub>IN</sub>	<b>Function</b>
		<p><b>Component Y Signal Input or RGB Signal Input</b>                      Pin to input component Y signals or RGB signals                      Select an input type (clamp/bias) with the Clamp/Bias pin (13pin) or I<sup>2</sup>C BUS.</p> <p>Note : As shown below, select an external input capacitance corresponding to an input type (clamp/bias).</p> <p>Pin voltage : 1.4V typ. [Clamp] [at Single mode]                      or 2.5V typ. [Bias] [at Single mode]                      Input impedance : 150kΩ [Bias]</p>
		<b>External circuit</b>
		<b>Input signal</b>
		<b>Equivalent circuit diagram</b>
		
		<p>Component Y signal input [Clamp select]      RGB signal input [Bias select]</p> <p>when not using it : Open</p>
		<p>Component Y signal</p>  <p>1V 0.6V Ternary synchronizing signal</p>
		<p>RGB signal</p>  <p>0.7V</p>

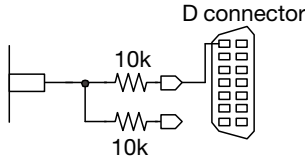
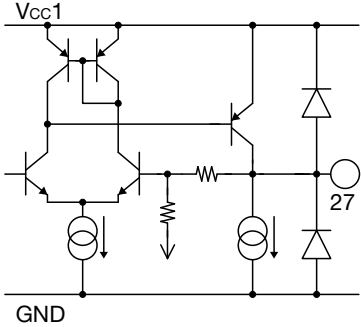
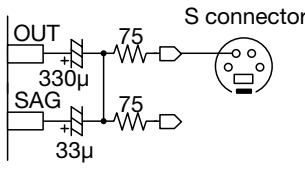
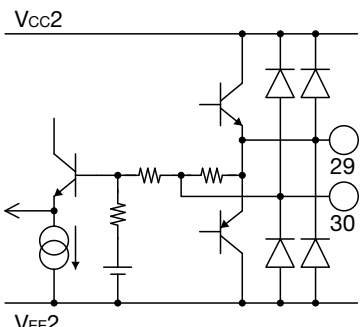
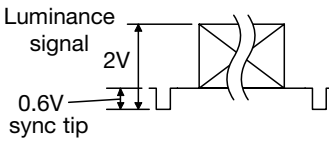
Pin No.	Pin name	Pin description	
13	Clamp/Bias	<b>Function</b>	
		<p>Clamp/Bias select                      Select an input type (clamp/bias) of CY<sub>IN</sub> (12pin) with a voltage applied to this pin.</p> <p>To select clamp or bias, I<sup>2</sup>C BUS can be also used.                      * See section Switch Control Table.</p> <p>Threshold : 1.4V typ.                      Input impedance : 40kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<p>when not using it : Open</p>	
		<b>Input signal</b>	
14	Cb <sub>IN</sub>	<b>Function</b>	
		<p>Color Difference Signal Cb Input or RGB Signal Input                      Pin to input color difference signals Cb or RGB signals.                      Bias input pin.</p> <p>Pin voltage : 2.5V typ. [at Single mode]                      Input impedance : 150kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<p>when not using it : Open</p>	
		<b>Input signal</b>	
		<p>Color difference signal</p> <p>Ternary synchronizing signal</p> <p>RGB signal</p>	

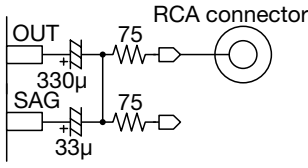
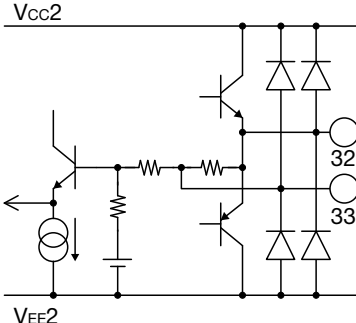
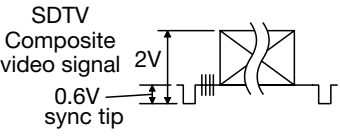
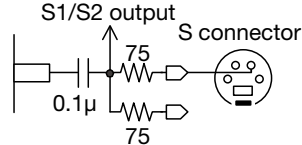
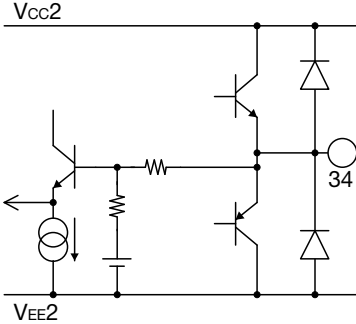
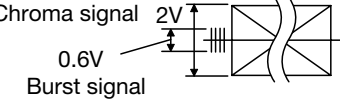
Pin No.	Pin name	Pin description	
15	SD/HD	<b>Function</b>	
		<p>LPF select</p> <p>Select a cutoff frequency of LPF (CY/Cb/Cr) with a voltage applied to this pin. (SD : pass bandwidth 13.5MHz / HD : pass bandwidth 30MHz)</p> <p>To select LPF, I<sup>2</sup>C BUS can be also used. ★ See section Switch Control Table.</p> <p>Threshold : 1.4V typ. Input impedance : 40kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<p style="text-align: center;"><b>Input signal</b></p> <p>DC Voltage : 0V(GND) to 5V(Vcc)</p>	
16	Cr <sub>IN</sub>	<b>Function</b>	
		<p>Color Difference Signal Cr Input or RGB Signal Input</p> <p>Pin to input color difference signals Cr or RGB signals.</p> <p>Bias input pin.</p> <p>Pin voltage : 2.5V typ. [at Single mode] Input impedance : 150kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<p style="text-align: center;"><b>Input signal</b></p> <p>Color difference signal</p>  <p>Ternary synchronizing signal</p> 	
			

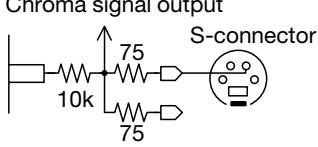
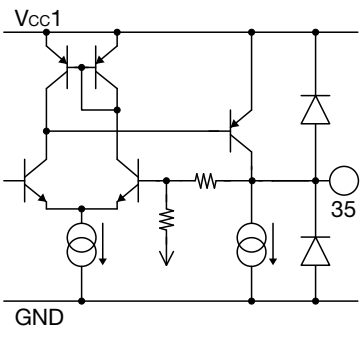
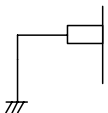
Pin No.	Pin name	Pin description	
18 21 24 31	V <sub>EE1</sub> V <sub>EE2</sub> V <sub>EE2</sub> V <sub>EE2</sub>	<b>Function</b>	
		<p>Negative Voltage Supply                      Pin to apply a negative supply voltage.                      Connect to GND when using a single power supply.                      Apply -3V when using dual power supplies.                      18pin is not shorted to 21pin, 24pin, or 31pin inside the IC.                      21pin, 24pin and 31pin are shorted inside the IC.                      V<sub>EE2</sub> is connected to an output stage circuit, and V<sub>EE1</sub> is connected to a circuit other than an output stage circuit.</p> <p>Note : Please arrange power supply bypass capacitor near the terminal when using dual power supplies.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			—
		<b>Input signal</b>	
		<p>DC Voltage :                      GND [at Single mode]                      -3.3V~ -2.7V [at Dual mode]</p>	
19	Crout	<b>Function</b>	
		<p>Color Difference Signal Cr Output or RGB Signal Output                      Pin to output color difference signals Cr or RGB signals.                      Bias output pin.</p> <p>Pin voltage: 2.4V typ. [at Single mode] or 0V typ. [at Dual mode]                      Output dynamic range: 3.0V<sub>P-P</sub> typ.                      * See section Pin Description Supplemental. 2, 3</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>	
		<p>Color difference signal</p>  <p>Ternary synchronizing signal</p>  <p>RGB signal</p> 	

Pin No.	Pin name	Pin description
20	Line3 out	<b>Function</b>
		<p>Line3 Output                      Pin to output Line3 of D connector detect signal                      The output DC voltage is controlled with I<sup>2</sup>C BUS.</p> <p>★ See section Switch Control Table.</p>
		<b>External circuit</b>
		<b>Input signal</b>
		<p>DC Voltage : 0V typ.                      or 2.1V typ.                      or 4.6V typ.</p>
		<b>Equivalent circuit diagram</b>
		
22	Cbout	<b>Function</b>
		<p>Color Difference Signal Cb Output or RGB Signal Output                      Pin to output color difference signals Cb or RGB signals.                      Bias output pin.</p> <p>Pin voltage : 2.4V typ. [at Single mode] or 0V typ. [at Dual mode]                      Output dynamic range : 3.0V<sub>P-P</sub> typ.</p> <p>★ See section Pin Description Supplemental. 2, 3</p>
		<b>External circuit</b>
		<b>Input signal</b>
		<p>Color difference signal</p>  <p>Ternary synchronizing signal</p> <p>RGB signal</p> 

Pin No.	Pin name	Pin description
23	Line2 out	<b>Function</b>
		<p>Line2 Output Pin to output Line2 of D connector detect signal. The output DC voltage is controlled with I<sup>2</sup>C BUS.</p> <p>★ See section Switch Control Table.</p>
		<b>External circuit</b>
		<b>Input signal</b>
		DC Voltage : 0V typ. or 4.6V typ.
		<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p> 
25 26	CY <sub>SAG</sub> CY <sub>OUT</sub>	<b>Function</b>
		<p>Component Y Signal Output or RGB Signal Output Pin to output component Y signals or RGB signals Select an output type (clamp/bias) with the Clamp/Bias pin (13pin) or I<sup>2</sup>C BUS.</p> <p>Pin voltage : 1.1V typ. [Clamp] [at Single mode] or 2.4V typ. [Bias] [at Single mode] or 0V typ. [at Dual mode]</p> <p>Output dynamic range : 2.8V<sub>P-P</sub> typ. [Clamp] or 3.0V<sub>P-P</sub> typ. [Bias]</p> <p>★ See section Pin Description Supplemental. 2, 3</p>
		<b>External circuit</b>
		<b>Input signal</b>
		<p>Component Y signal</p>  <p>Ternary synchronizing signal</p> <p>RGB signal</p> 
		<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p> 

Pin No.	Pin name	Pin description	
27	Line1 out	<b>Function</b>	
		<p>Line1 Output                      Pin to output Line1 of D connector detect signal.                      The output DC voltage is controlled with I<sup>2</sup>C BUS.</p> <p>* See section Switch Control Table.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
<b>Input signal</b>			
		DC Voltage : 0V typ. or 2.1V typ. or 4.6V typ.	
29 30	Y <sub>OUT</sub> Y <sub>SAG</sub>	<b>Function</b>	
		<p>Luminance Signal Output                      Pin to output luminance signals of S-video.                      Clamp output pin.</p> <p>Pin voltage : 1.1V typ. [at Single mode] or 0V typ. [at Dual mode]                      Output dynamic range : 2.8V<sub>P-P</sub> typ.</p> <p>* See section Pin Description Supplemental. 2, 3</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
<b>Input signal</b>			
			

Pin No.	Pin name	Pin description	
32 33	V <sub>OUT</sub> V <sub>SAG</sub>	<b>Function</b>	
		<p>Composite Video Signal Output Pin to output composite video signals. Clamp output pin.</p> <p>Pin voltage : 1.1V typ. [at Single mode] or 0V typ. [at Dual mode] Output dynamic range : 2.8V<sub>P-P</sub> typ.</p> <p>★ See section Pin Description Supplemental. 2, 3</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<b>Input signal</b>	
			
34	C <sub>OUT</sub>	<b>Function</b>	
		<p>Chroma Signal Output Pin to output Chrominance signals of S-video. Bias output pin.</p> <p>Pin voltage : 2.4V typ. [at Single mode] or 0V typ. [at Dual mode] Output dynamic range : 3.0V<sub>P-P</sub> typ.</p> <p>★ See section Pin Description Supplemental. 2, 3</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>when not using it : Open</p>	
		<b>Input signal</b>	
			

Pin No.	Pin name	Pin description	
35	S1/S2 out	<b>Function</b>	
		<p>S1/S2 Output                      Pin to output S1/S2 of S-connector detect signal.                      The output DC voltage is controlled with I<sup>2</sup>C BUS.</p> <p>★ See section Switch Control Table.</p> <p>Output Impedance : 200Ω typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<p>Chroma signal output</p>  <p>when not using it : Open</p>	
		<b>Input signal</b>	
<p>DC Voltage : 0V typ.                      or 2.1V typ.                      or 4.6V typ.</p>			
36	GND	<b>Function</b>	
		<p>Ground                      Ground pin.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			—
		<b>Input signal</b>	
—			

Supplemental 1 : SAG pin

If the SAG pin is not used, the OUT pin and the SAG pin should be shorted.  
 Then, a coupling capacitance of approx. 1000μF should be used.

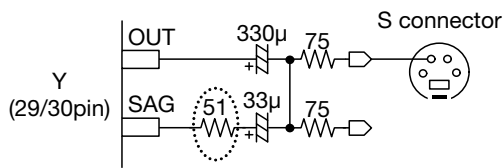
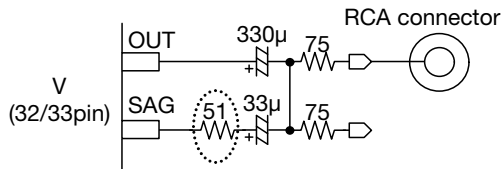
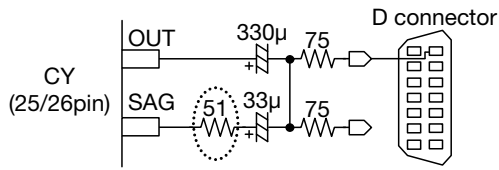
Supplemental 2 : Using dual power supplies

When using dual power supplies, the device level shifts so that the pedestal level outputs with 0±0.1V (no signal : 0±0.1V) if sending a signal of the pedestal level of 0.3V (no signal : 0.3V) to a terminal where the luminance elements of V<sub>IN</sub>, Y<sub>IN</sub>, and CY<sub>IN</sub> are received, and sending a signal of the center of 0.6V (no signal : 0.6V) to a terminal where the color elements of C<sub>IN</sub>, C<sub>bIN</sub>, C<sub>rIN</sub> are received. Thus, the output coupling capacitance can be eliminated.

Supplemental3 : Wire routing for video output pins

Keep the wire as short as possible between each video output pin and 75Ω.

If using a SAG correction circuit, when wire routing is long, add a resistor as shown below.



Supplemental 4 : D connector discernment signal output pin

Object : S1/S2 out (35pin) , Line1 out (27pin) , Line2 out (23pin) , Line3 out (20pin)

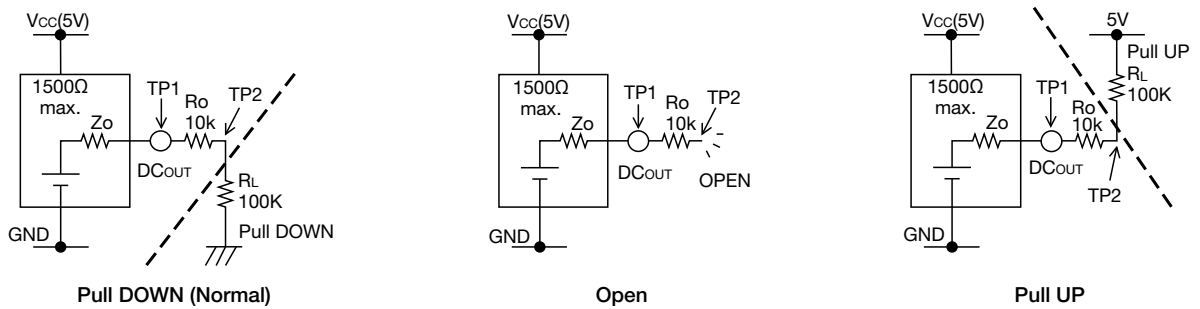
The output impedance of these terminals of MM1757FH is 1500Ω max. (Refer to electrical characteristics) .

There is a case where D connector specification (CP-4120) is not fulfilled depending on the state of connection apparatus.

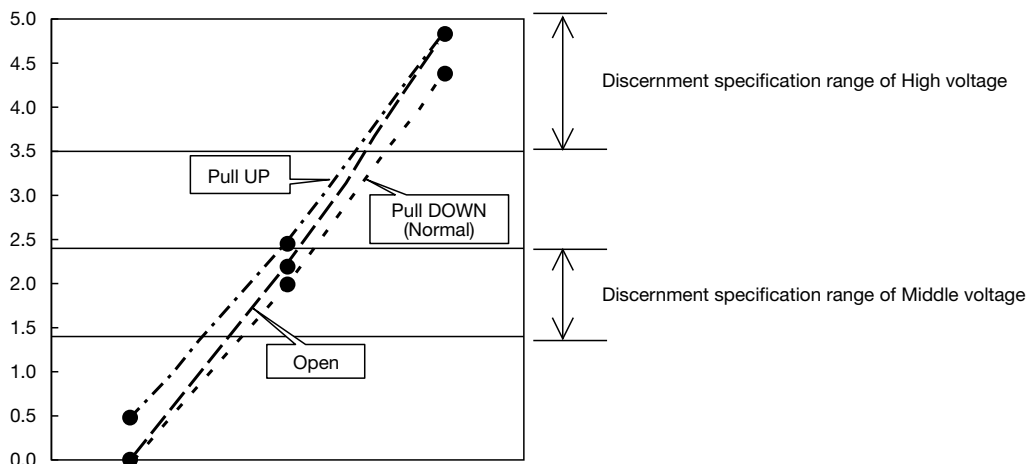
In this case, please adjust the value of the external series resistance  $R_o$ .

D connector discernment signal line specifications			The example of Output Voltage ( $R_o=10k\Omega$ , $R_L=Open$ or $100k\Omega$ )						
Discernment voltage	Tolerance		Pull DOWN (Normal)		OPEN		Pull UP		UNIT
			TP1	TP2	TP1	TP2	TP1	TP2	
H	5.0	0 -1.5	4.82	4.38	4.84	4.83	4.84	4.85	V
M	2.2	+0.2 -0.8	2.19	1.99	2.19	2.19	2.19	2.45	V
L	0		0	0	0	0	0.03	0.48	V

Measurement circuit diagram \* TP=Test Point



Graph Output voltage TP2



**Absolute Maximum Ratings** (at the single power supply , except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG_S</sub>	-55~+150	°C
Operating temperature	T <sub>OPR_S</sub>	-40~+85	°C
Supply voltage	V <sub>CC max_S</sub>	6	V
Allowable loss (Note1)	Pd <sub>S</sub>	2.6	W

Note1 : Board mounting allowable loss. Board size 100 × 100 × 1.6mm

**Absolute Maximum Ratings** (at the dual power supply, except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG_d</sub>	-55~+150	°C
Operating temperature	T <sub>OPR_d</sub>	-40~+85	°C
Positive supply voltage	V <sub>CC max_d</sub>	6	V
Negative supply voltage	V <sub>EE max_d</sub>	-4	V
Allowable loss (Note2)	Pd <sub>d</sub>	2.6	W

Note2 : Board mounting allowable loss. Board size 100 × 100 × 1.6mm

**Recommended Operating Conditions** (at the single power supply)

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR_S</sub>	-40~+85	°C
Operating voltage	V <sub>CCOP_S</sub>	4.5~5.5	V

**Recommended Operating Conditions** (at the dual power supply)

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR_d</sub>	-40~+75	°C
Positive operating voltage	V <sub>CCOP_d</sub>	4.7~5.3	V
Negative operating voltage	V <sub>EEOP_d</sub>	-2.7~-3.3	V

**Electrical Characteristics** (at the single power supply, except where noted otherwise, Ta=25°C, Vcc=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
Supply current 1	Icc1_s	No signal	87	125	162	mA	
Supply current 2	Icc2_s	No signal, Mute1 : ON	66	95	123	mA	
Supply current 3	Icc3_s	No signal, Mute2 : ON	35	50	65	mA	
Supply current 4	Icc4_s	No signal, Mute1 and Mute2 : ON	6	9	12	mA	
Terminal voltage	Chroma input	V <sub>CIN_s</sub>	1pin	2.0	2.5	3.0	V
	Composite video input	V <sub>VIN_s</sub>	3pin	1.2	1.4	1.6	V
	Luminance input	V <sub>YIN_s</sub> , C <sub>YIN_s</sub>	5, 12pin	1.2	1.4	1.6	V
	Component input	V <sub>CbIn_s</sub> , C <sub>CrIn_s</sub>	14, 16pin	2.0	2.5	3.0	V
	Chroma output	V <sub>COUt_s</sub>	34pin		2.4		V
	Composite video output	V <sub>VOUt_s</sub>	32pin		1.1		V
	Luminance output	V <sub>YOUt_s</sub> , C <sub>YOUt_s</sub>	26, 29pin		1.1		V
Component output	V <sub>CbOut_s</sub> , C <sub>CrOut_s</sub>	19, 22pin		2.4		V	
Output dynamic range	DR3, 5, 7, 8_s (★ 6)	SIN wave : 100kHz, THD=1.0%	2.6	3.0		V	
	DR1, 2, 4, 6_s (★ 6)	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V	

**Electrical Characteristics** (at the dual power supply, except where noted otherwise, Ta=25°C, Vcc=5V, VEE=-3V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
Positive supply current 1	Icc1_d	No signal	87	125	162	mA	
Positive supply current 2	Icc2_d	No signal, Mute1 : ON	66	95	123	mA	
Positive supply current 3	Icc3_d	No signal, Mute2 : ON	35	50	65	mA	
Positive supply current 4	Icc4_d	No signal, Mute1 and Mute2 : ON	6	9	12	mA	
Negative supply current 1	IEE1_d	No signal	80	115	150	mA	
Negative supply current 2	IEE2_d	No signal, Mute1 : ON	60	85	110	mA	
Negative supply current 3	IEE3_d	No signal, Mute2 : ON	28	40	52	mA	
Negative supply current 4	IEE4_d	No signal, Mute1 and Mute2 : ON		1	4	mA	
Terminal voltage	Chroma output	V <sub>COUt_d</sub>	34pin (★ 1)	-0.18	0.0	0.18	V
	Composite video output	V <sub>VOUt_d</sub>	32pin (★ 2)	-0.18	0.0	0.18	V
	Luminance output	V <sub>YOUt_d</sub> , C <sub>YOUt_d</sub>	26, 29pin (★ 3)	-0.18	0.0	0.18	V
	Component output	V <sub>CbOut_d</sub> , C <sub>CrOut_d</sub>	19, 22pin (★ 4)	-0.18	0.0	0.18	V
Output dynamic range	DR3, 5, 7, 8_d (★ 6)	SIN wave : 100kHz, THD=1.0%	3.0			V	
	DR1, 2, 4, 6_d (★ 6)	SIN wave : 100kHz, THD=1.0%	3.0			V	

**Electrical Characteristics**

(Except where noted otherwise Ta=25°C, VCC=5V, VEE=-3V [dual power supply] or VCC=5V [single power supply])

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Control terminal input voltage	High V <sub>thHm</sub> (★ 5)	2, 4, 6, 13, 15, 17pin	2.1			V
	Low V <sub>thLm</sub> (★ 5)				0.7	V
Control terminal input current	High I <sub>Hm</sub> (★ 5)	2, 4, 6, 13, 15, 17pin, V <sub>H</sub> =4.5V			160	μA
	Low I <sub>Lm</sub> (★ 5)	2, 4, 6, 13, 15, 17pin, V <sub>L</sub> =0.4V			15	μA
Address threshold voltage	90H V <sub>th90</sub>	10pin			0.8	V
	92H V <sub>th92</sub>		2.2			V
S1/S2 out Terminal output voltage	High V <sub>SoutH</sub>	R <sub>L</sub> =10kΩ+100kΩ	4.3	4.6		V
	Middle V <sub>SoutM</sub>	R <sub>L</sub> =10kΩ+100kΩ	1.6	2.1	2.4	V
	Low V <sub>SoutL</sub>	R <sub>L</sub> =10kΩ+100kΩ		0.1	0.5	V
Line1 out Terminal output voltage	High V <sub>L1outH</sub>	R <sub>L</sub> =10kΩ+100kΩ	4.3	4.6		V
	Middle V <sub>L1outM</sub>	R <sub>L</sub> =10kΩ+100kΩ	1.6	2.1	2.4	V
	Low V <sub>L1outL</sub>	R <sub>L</sub> =10kΩ+100kΩ		0.1	0.5	V
Line2 out Terminal output voltage	High V <sub>L2outH</sub>	R <sub>L</sub> =10kΩ+100kΩ	4.3	4.6		V
	Low V <sub>L2outL</sub>	R <sub>L</sub> =10kΩ+100kΩ		0.1	0.5	V
Line3 out Terminal output voltage	High V <sub>L3outH</sub>	R <sub>L</sub> =10kΩ+100kΩ	4.3	4.6		V
	Middle V <sub>L3outM</sub>	R <sub>L</sub> =10kΩ+100kΩ	1.6	2.1	2.4	V
	Low V <sub>L3outL</sub>	R <sub>L</sub> =10kΩ+100kΩ		0.1	0.5	V
Input impedance	Z <sub>CIN</sub> , C <sub>IN</sub> , C <sub>TIN</sub>	1, 14, 16pin	100	150	200	kΩ
Output impedance	Z <sub>SOUT</sub> , L <sub>1OUT</sub> , L <sub>2OUT</sub> , L <sub>3OUT</sub>	20, 23, 27, 35pin		200		Ω
Voltage gain	G <sub>1n</sub> (★ 6)	SIN wave : 1V, f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic 1 (C, V, Y)	f <sub>1-5</sub> (★ 6)	SIN wave : 1V, 6.75MHz/100kHz	-1.0	0.0	1.0	dB
	f <sub>21-5</sub> (★ 6)	SIN wave : 1V, 27MHz/100kHz		-33	-27	dB
Frequency characteristic 2 (CY, Cb, Cr) at Standard Definition select	f <sub>36-8</sub> (★ 6)	SIN wave : 1V, 13.5MHz/100kHz	-1.0	0.0	1.0	dB
	f <sub>46-8</sub> (★ 6)	SIN wave : 1V, 54MHz/100kHz		-33	-27	dB
Frequency characteristic 3 (CY, Cb, Cr) at High Definition select	f <sub>56-8</sub> (★ 6)	SIN wave : 1V, 30MHz/100kHz	-1.0	0.0	1.0	dB
	f <sub>66-8</sub> (★ 6)	SIN wave : 1V, 74MHz/100kHz		-33	-27	dB
Group delay 1	t <sub>1GD1-5</sub> (★ 6)	at 100kHz		45	80	ns
Group delay 2	t <sub>2GD6-8</sub> (★ 6)	Standard Definition select at 100kHz		25	50	ns
Group delay 3	t <sub>2GD6-8</sub> (★ 6)	High Definition select at 100kHz		22	45	ns
Group delay deviation 1 (C, V, Y)	Δt <sub>1GD1-5</sub> (★ 6)	to 3.58MHz		4	10	ns
		to 4.43MHz		6	10	ns
		to 6MHz		12	20	ns
Group delay deviation 2 (CY, Cb, Cr) at Standard Definition select	Δt <sub>2GD6-8</sub> (★ 6)	to 2MHz		1	10	ns
		to 12MHz		6	15	ns
Group delay deviation 3 (CY, Cb, Cr) at High Definition select	Δt <sub>3GD6-8</sub> (★ 6)	to 4MHz		1	10	ns
		to 24MHz		6	15	ns
Between channel Group delay deviation 1	Δt <sub>1chGD</sub>	Between C and Y at 3.58MHz		1	10	ns
Between channel Group delay deviation 2	Δt <sub>2chGD</sub>	Between CY and Cb (Cr) at 2MHz (Standard Definition)		1	10	ns
Between channel Group delay deviation 3	Δt <sub>3chGD</sub>	Between CY and Cb (Cr) at 4MHz (High Definition)		1	10	ns
Differential gain	DG <sub>1-3</sub> (★ 6)	Staircase signal 1V		1.0	1.5	%
Differential phase	DP <sub>1-3</sub> (★ 6)	Staircase signal 1V		1.0	1.5	°
Crosstalk 1	CT <sub>1n</sub> (★ 6)	f=4.43MHz, 1V		-60	-55	dB
Crosstalk 2	CT <sub>2n</sub> (★ 6)	f=20MHz, 1V		-45	-40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
S/N 1	SN <sub>1,4-5</sub> (* 6)	BW : 100k ~ 6MHz		-80		dB
S/N 2	SN <sub>2-3</sub> (* 6)	BW : 100k ~ 6MHz at MIX OUT		-74		dB
S/N 3	SN <sub>3,6-8</sub> (* 6)	BW : 100k ~ 6MHz at SD select		-80		dB
S/N 4	SN <sub>4,6-8</sub> (* 6)	BW : 100k ~ 30MHz at HD select		-66		dB

Note1 : \* 1 It is a output terminal voltage when input terminal (1pin) is 0.6V.  
 Note2 : \* 2 It is a output terminal voltage when input terminal (3pin) is 0.3V.  
 Note3 : \* 3 It is a output terminal voltage when input terminal (5, 12pin) is 0.3V.  
 Note4 : \* 4 It is a output terminal voltage when input terminal (14, 16pin) is 0.6V.  
 Note5 : \* 5 The subscript number "m" is the terminal of under table.

m	terminal
1	Mute1
2	Mute2
3	SD/HD
4	YC MIX
5	Clamp/Bias
6	Dual/Single

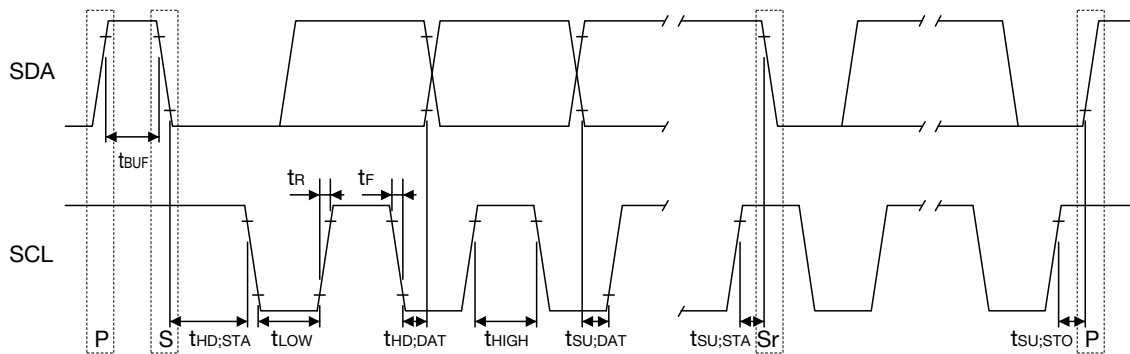
Note6 : \* 6 The subscript number "n" is the combination of under table.

n	input	output
1	V <sub>IN</sub>	V <sub>OUT</sub>
2	Y <sub>IN</sub>	
3	C <sub>IN</sub>	
4	Y <sub>IN</sub>	Y <sub>OUT</sub>
5	C <sub>IN</sub>	C <sub>OUT</sub>
6	CY <sub>IN</sub>	CY <sub>OUT</sub>
7	Cb <sub>IN</sub>	Cb <sub>OUT</sub>
8	Cr <sub>IN</sub>	Cr <sub>OUT</sub>

**Electrical Characteristics** (Except where noted otherwise  $T_a=25^\circ\text{C}$ ,  $V_{CC}=5\text{V}$ ,  $V_{EE}=-3\text{V}$  [dual power supply] or  $V_{CC}=5\text{V}$  [single power supply])

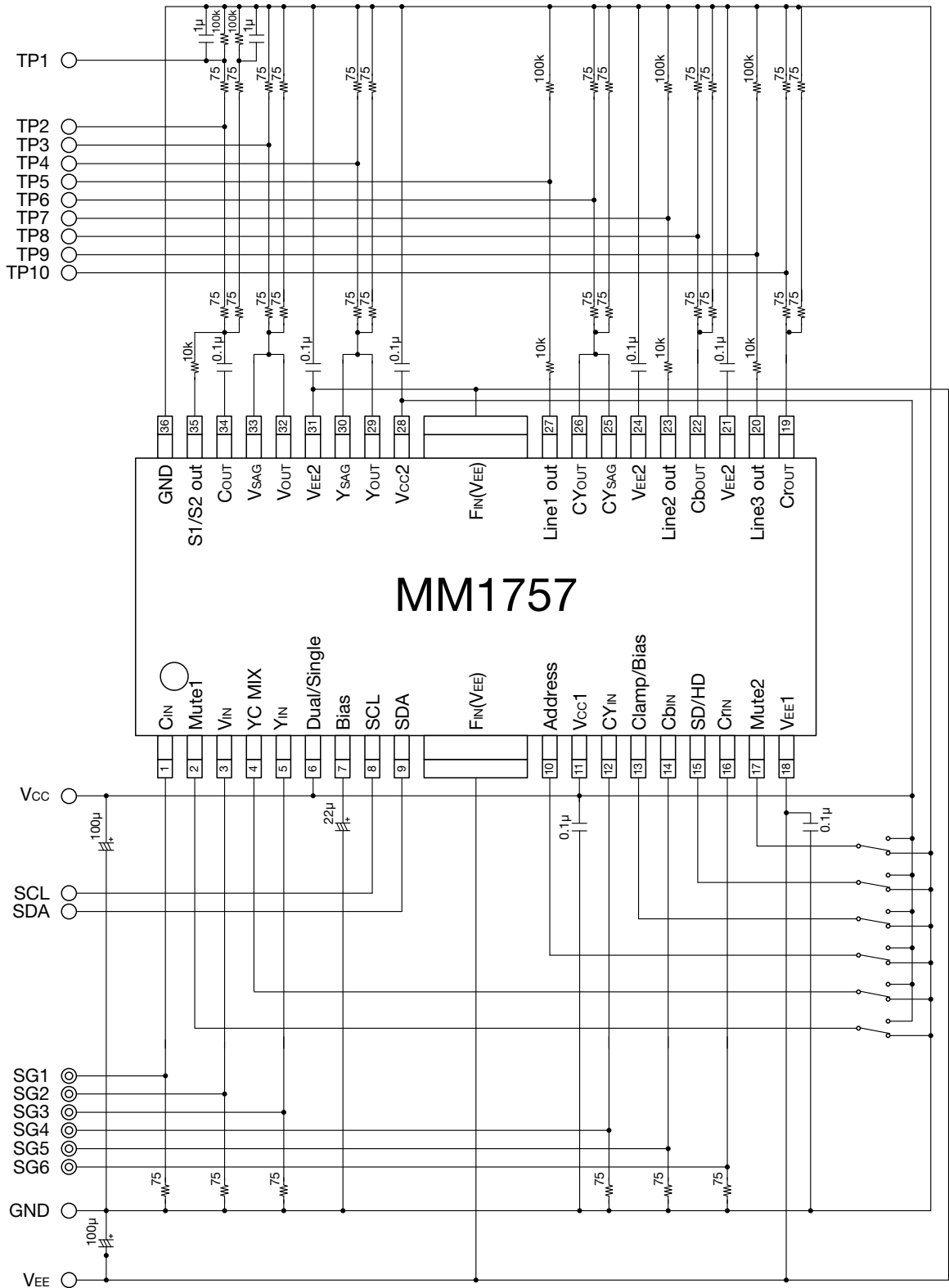
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[ I <sup>2</sup> C condition]						
Input voltage Low	V <sub>IL</sub>		0		0.7	V
Input voltage High	V <sub>IH</sub>		2.1		5.0	V
SDA low level output voltage	V <sub>OL</sub>	SDA sink 3mA	0		0.4	V
High level input current	I <sub>IH</sub>	SDA, SCL=4.5V	-10		10	μA
Low level input current	I <sub>IL</sub>	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f <sub>SCL</sub>				100	kHz
Data transfer wait time	t <sub>BUF</sub>		4.7			μs
SCL start hold time	t <sub>HD;STA</sub>		4.0			μs
SCL low level hold time	t <sub>LOW</sub>		4.7			μs
SCL high level hold time	t <sub>HIGH</sub>		4.0			μs
Start condition setup time	t <sub>SU;STA</sub>		4.7			μs
SDA data hold time	t <sub>HD;DAT</sub>		0			μs
SDA data setup time	t <sub>SU;DAT</sub>		250			ns
SDA, SCL rise time	t <sub>R</sub>				1000	ns
SDA, SCL fall time	t <sub>F</sub>				300	ns
Stop condition setup time	t <sub>SU;STO</sub>		4.0			μs

I<sup>2</sup>C condition

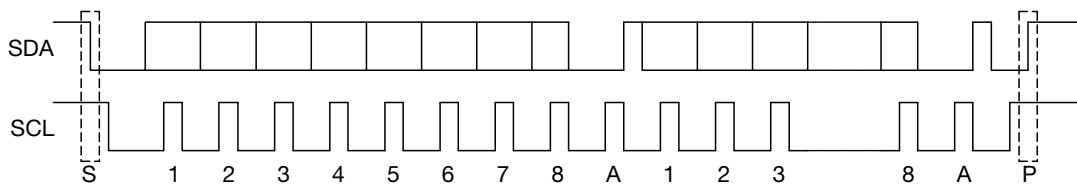




**Measuring Circuit** (at the dual power supply)



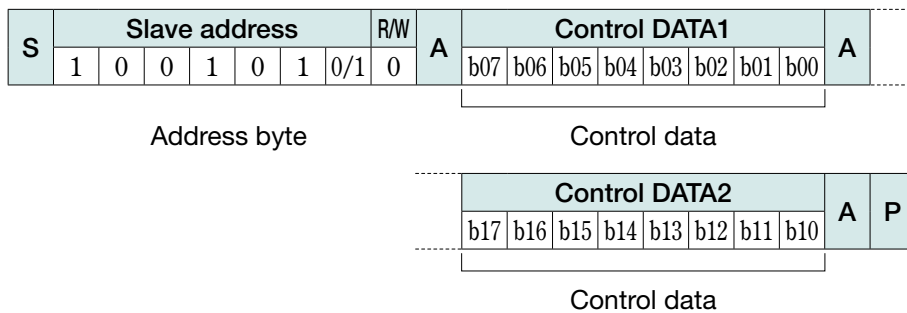
I<sup>2</sup>C BUS



I<sup>2</sup>C BUS is inter IC bus system controlled by 2 lines (SDA,SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used control register. As MM1757 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

No.	Control DATA condition							
Control DATA1	b07	b06	b05	b04	b03	b02	b01	b00
				SD/HD	YC MIX	Clamp/Bias	Mute1	Mute2
Control DATA2	b17	b16	b15	b14	b13	b12	b11	b10
		Line1		Line2	Line3		S1/S2	

MM1757 consists of one address byte and two control data bytes (3bytes in total). All data over the limited length (4th and subsequent bytes) is fully neglected.

For details of the control contents of switches, refer to the separate table.

■ Switch Control Table (\* : Don't care (High Low))

(1) Mute select

I <sup>2</sup> C control		Control terminal		Output terminal					
b01	b00	Mute1 (2pin)	Mute2 (17pin)	V <sub>OUT</sub>	Y <sub>OUT</sub>	C <sub>OUT</sub>	CY <sub>OUT</sub>	Cb <sub>OUT</sub>	Cr <sub>OUT</sub>
0	*	Low	*	Mute OFF			*	*	*
1		Low		Mute ON					
*		High							
*	0	*	Low	*	*	*	Mute OFF		
	1		Low				Mute ON		
	*		High						

(2) Clamp/Bias select

I <sup>2</sup> C control	Control terminal	Input terminal	
b02	Clamp/Bias (13pin)	CY <sub>IN</sub> (Single)	CY <sub>IN</sub> (Dual)
0	Low	Clamp ON	Clamp OFF
1	Low	Bias	
*	High		

(3) YC MIX select

I <sup>2</sup> C control	Control terminal	Input terminal
b03	YC MIX (4pin)	V <sub>OUT</sub>
0	Low	V <sub>IN</sub>
1	Low	Y <sub>IN</sub> + C <sub>IN</sub>
*	High	

.Single : Single power supply, Dual: Dual power supply

(1) + (2) + (3) Input select

Input	Output	I <sup>2</sup> C BUS Control				Control terminal				
		b03	b02	b01	b00	YC MIX (4pin)	Clamp/Bias (13pin)	Mute1 (2pin)	Mute2 (17pin)	
Mute	V <sub>OUT</sub>	*	*	1	*	*	*	Low	*	
				*				High		
0		Low								
1		High								
V <sub>IN</sub> + C <sub>IN</sub>		*		0						
Mute	Y <sub>OUT</sub>	*	*	1	*	*	*	Low	*	
				*				High		
Y <sub>IN</sub>		*		0				Low		
Mute	C <sub>OUT</sub>	*	*	1	*	*	*	Low	*	
				*				High		
C <sub>IN</sub>		*		0				Low		
Mute	CY <sub>OUT</sub>	*	*	*	1	*	*	Low	*	
										*
Y <sub>IN</sub> (Clamp ON or OFF)			*		0				Low	Low
Y <sub>IN</sub> (Bias)			*		1				Low	
Mute	Cb <sub>OUT</sub>	*	*	*	1	*	*	*	Low	
					*				High	
Cb <sub>IN</sub>		*		0				Low		
Mute	Cr <sub>OUT</sub>	*	*	*	1	*	*	*	Low	
					*				High	
Cr <sub>IN</sub>		*		0				Low		

LPF select

I <sup>2</sup> C control	Control terminal	CY, C <sub>B</sub> , C <sub>R</sub> LPF bandwidth
b04	SD/HD (15pin)	
0	Low	13.5MHz (Standard Definition)
1	Low	30MHz
*	High	(High Definition)

S1/S2 Output terminal voltage [Aspect]

I <sup>2</sup> C control		S1/S2 out Output voltage	Signal mode
b11	b10		
0	0	0V	4:3 Normal
0	1	2.1V	4:3 Letter box
1	1		
1	0	4.6V	16:9 Squeeze

Line1 Output terminal voltage [Scanning Line]

I <sup>2</sup> C control		Line1 out Output voltage	Signal mode
b16	b15		
0	0	0V	480
0	1	2.1V	720
1	1		
1	0	4.6V	1080

Line2 Output terminal voltage [Interlace/Progressive]

I <sup>2</sup> C control	Line2 out Output voltage	Signal mode
b14		
0	0V	Interlace
1	4.6V	Progressive

Line3 Output terminal voltage [Aspect]

I <sup>2</sup> C control		Line3 out Output voltage	Signal mode
b13	b12		
0	0	0V	4:3 Normal
0	1	2.1V	4:3 Letter box
1	1		
1	0	4.6V	16:9 Squeeze

Dual/Single power supply select

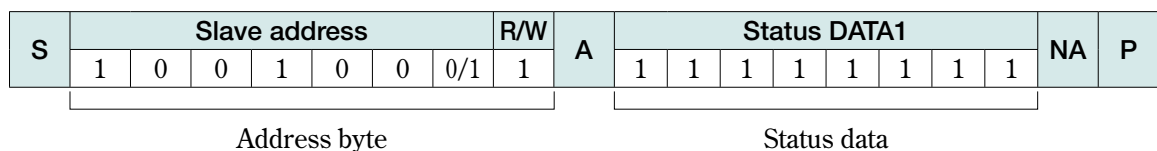
Control terminal	Power supply
Dual/Single (6pin)	
Low	Single
High	Dual

[Status registers]

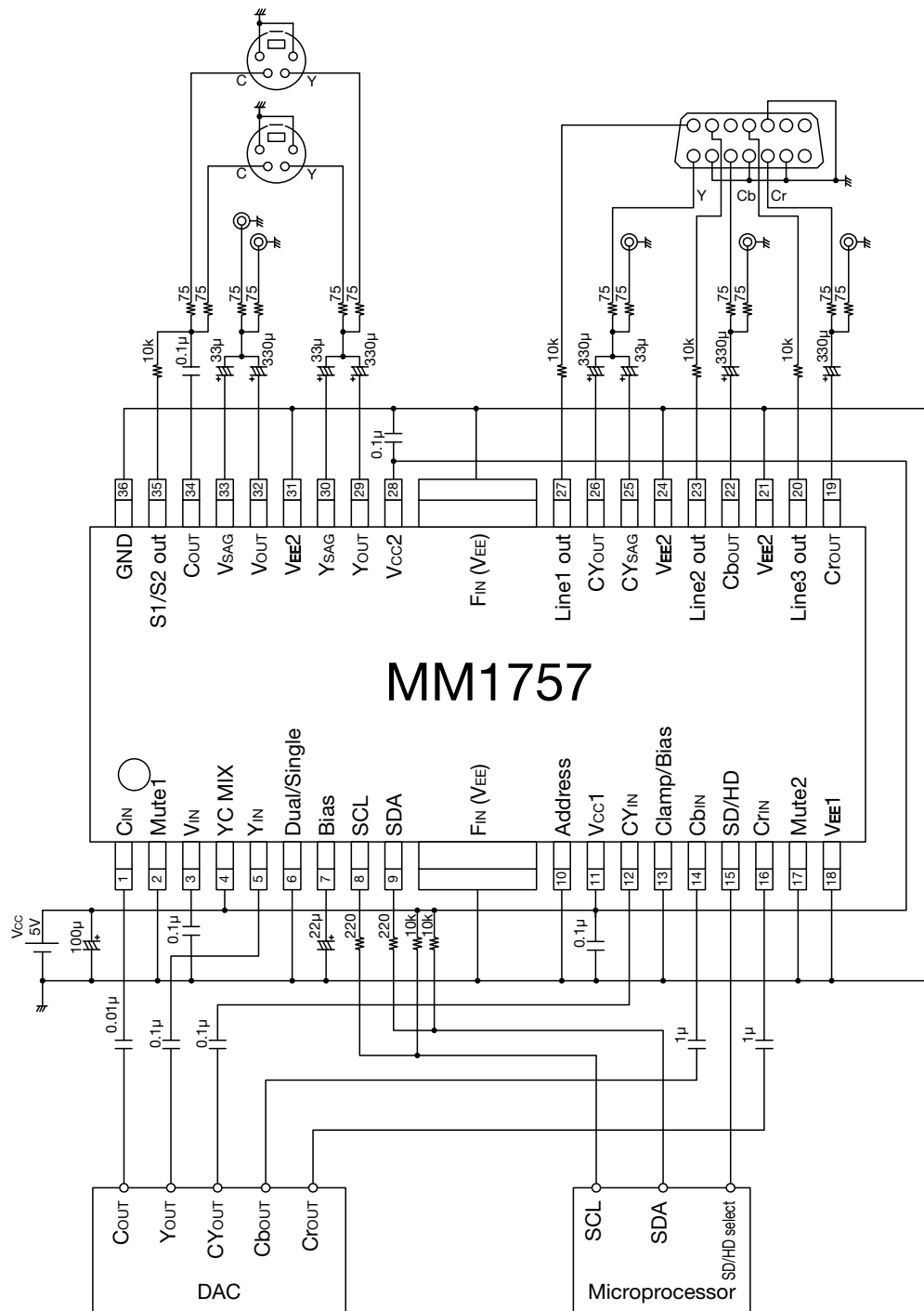
There is no preparation of the status register in MM1757.

A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.



Application Circuit 1 (at the single power supply)

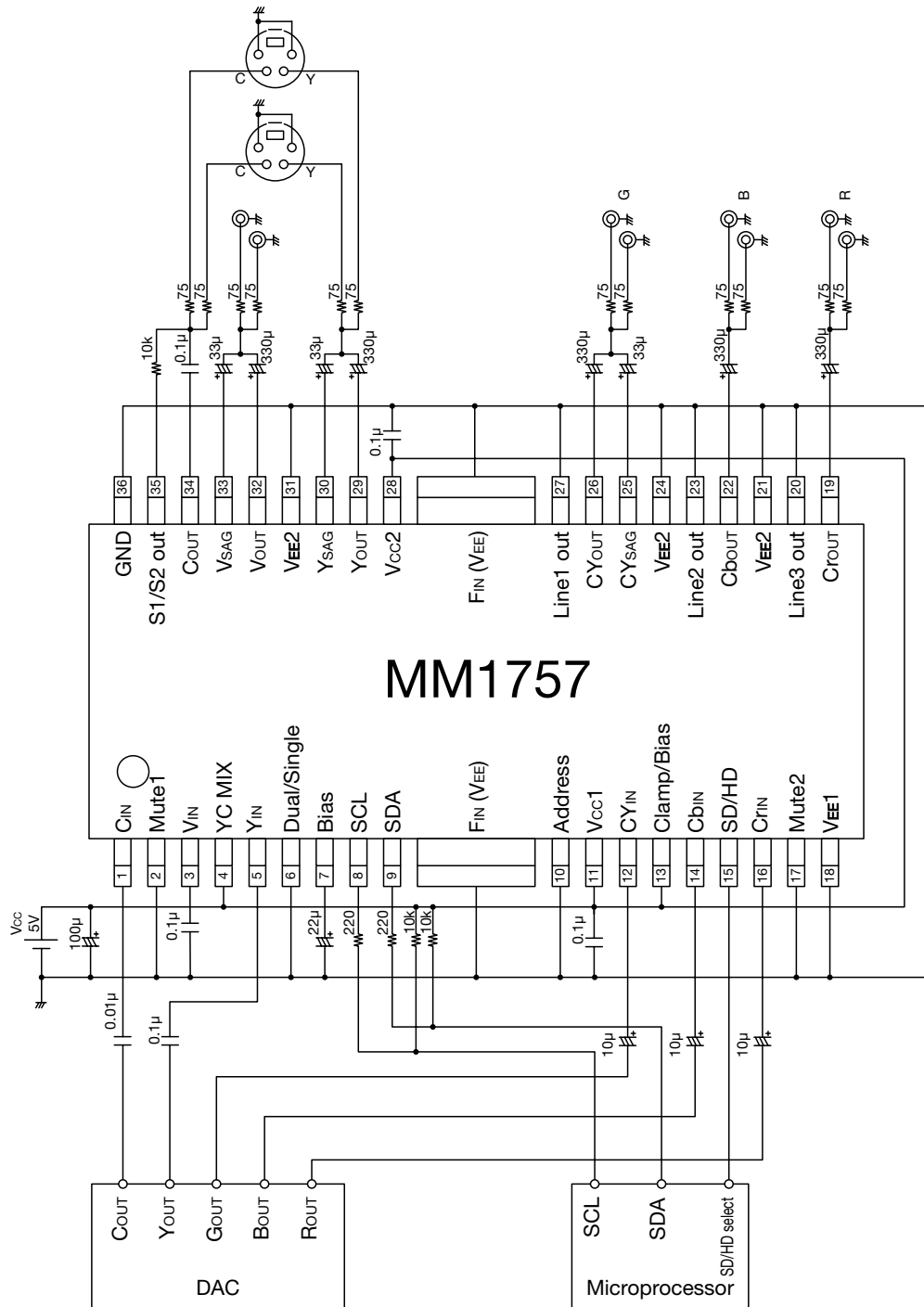


Note1: Please arrange power supply bypass capacitor near the V<sub>CC</sub> terminal (pin).

Note2: Please arrange the stray capacity component added to a signal output terminal to 20pF or less.



**Application Circuit 3** (When RGB signal is used)

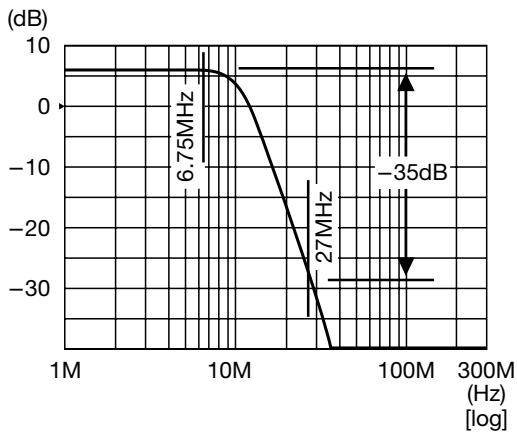


Note1: Please arrange power supply bypass capacitor near the V terminal (pin).

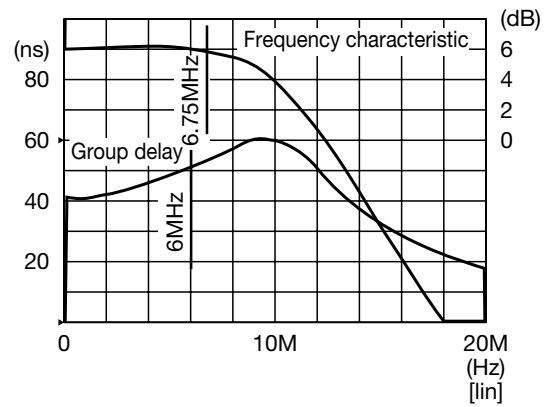
Note2: Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

## Characteristics

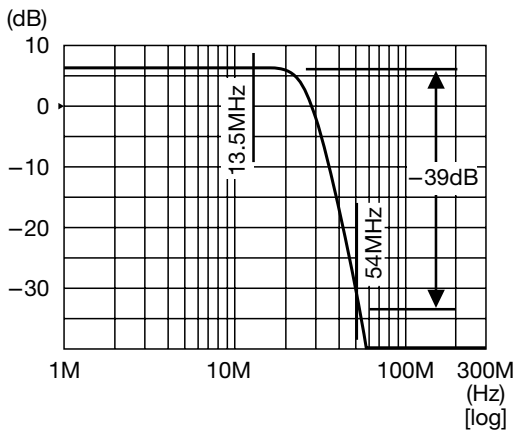
### Frequency characteristic (C<sub>OUT</sub>, V<sub>OUT</sub>, Y<sub>OUT</sub>)



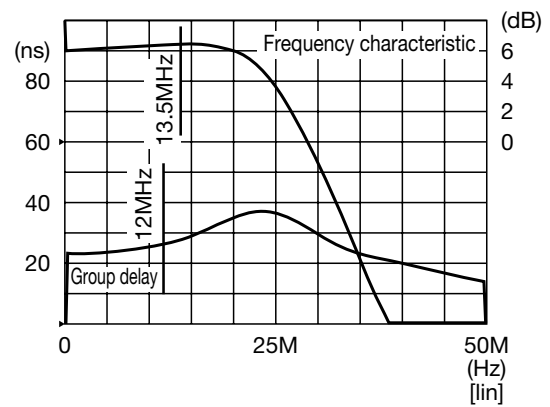
### Group delay (C<sub>OUT</sub>, V<sub>OUT</sub>, Y<sub>OUT</sub>)



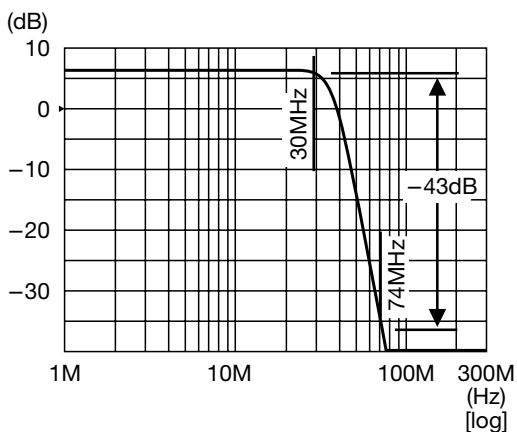
### Frequency characteristic (C<sub>YOUT</sub>, C<sub>bOUT</sub>, C<sub>rOUT</sub>) [at SD select]



### Group delay (C<sub>YOUT</sub>, C<sub>bOUT</sub>, C<sub>rOUT</sub>) [at SD select]



### Frequency characteristic (C<sub>YOUT</sub>, C<sub>bOUT</sub>, C<sub>rOUT</sub>) [at HD select]



### Group delay (C<sub>YOUT</sub>, C<sub>bOUT</sub>, C<sub>rOUT</sub>) [at HD select]

