

# IC for System Reset (with built-in watchdog timer) Monolithic IC MM1096

March 3, 2004

## Outline

This IC functions in a variety of CPU systems and other logic systems to generate a reset signal and reset the system accurately when the power is turned on or interrupted.

It includes a watchdog timer which allows diagnosis of the system operation, so that it prevents system runaway by intermittently generating a reset pulse when system misoperation occurs.

## Features

1. Built-in watchdog timer
2. Low current consumption 130 $\mu$ A typ.
3. Low operating limit voltage  $V_{CC}=0.8V$
4. Watch dog stop function (RCT pin) included
5. Long clock monitoring time  
 $T_{PR}$  (POWER ON) :  $T_{WD}$  (clock monitoring)=1 : 5
6. Fewer outer components

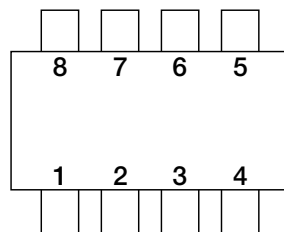
## Packages

- DIP-8B (MM1096AD, MM1096BD)
- SOP-8C (MM1096AF, MM1096BF)

## Applications

1. Reset circuits for microcomputers, CPUs and MPUs
2. Reset circuits for logic circuits
3. Microcomputer system monitoring, etc.

## Pin Assignment



DIP-8B/SOP-8C  
(TOP VIEW)

1	TC
2	NC
3	CK
4	GND
5	$V_{CC}$
6	RCT
7	$V_S$
8	$\overline{\text{RESET}}$

**Pin Description**

Pin No.	Pin name	Function
1	TC	T <sub>WD</sub> , T <sub>WR</sub> , T <sub>PR</sub> variable pins. (T <sub>WD</sub> , T <sub>WR</sub> and T <sub>PR</sub> times are determined by the external capacitor.) T <sub>PR</sub> (ms) = 500 × C <sub>T</sub> (μF) T <sub>WD</sub> (ms) = 2500 × C <sub>T</sub> (μF) T <sub>WR</sub> (ms) = 100 × C <sub>T</sub> (μF)
2	N.C	
3	CK	Clock input pin, inputs clock from logic system
4	GND	GND pin
5	V <sub>CC</sub>	Voltage detection MM1096A → 3.2V, MM1096B → 4.2V
6	RCT	Watchdog timer stop pin Operation modes : Operation → OPEN, Stop → connect to GND
7	V <sub>S</sub>	Detection voltage variable pin
8	RESET	Reset output pin (low output)

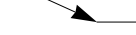


**Absolute Maximum Ratings**

Item	Symbol	Rating	Units
Power supply voltage	V <sub>CC</sub> max.	-0.3~+10	V
CK pin input voltage	V <sub>CK</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +10)	V
V <sub>S</sub> pin input voltage	V <sub>VS</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +10)	V
Voltage applied to RCT pin	V <sub>RCT</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +10)	V
Voltage applied to RESET pin	V <sub>OH</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +10)	V
Allowable loss	P <sub>d</sub>	300	mW
Storage temperature	T <sub>STG</sub>	-40~+125	°C

**Recommended Operating Conditions**

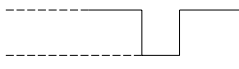


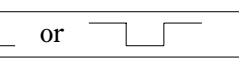
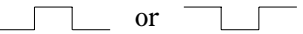


Item	Symbol	Rating	Units
Supply Voltage	V <sub>CC</sub>	+2.2~+7.0	V
RESET Sink Current	I <sub>OL</sub>	0~1.0	mA
Watchdog Time Monitoring Time Set value	T <sub>WD</sub>	0.1~5000	ms
Reset Hold Time at Power Rise Set value	T <sub>PR</sub>	0.1~5000	ms
Clock Rise and Fall Time	t <sub>rc</sub> , t <sub>fc</sub>	<100	μs
Operating Temperature	T <sub>OP</sub>	-25~+75	°C

**Electrical Characteristics (DC)** (Except where noted otherwise, MM1096A :  $V_{CC}=3.6V$ ,  $T_a=25^{\circ}C$ , MM1096B :  $V_{CC}=5.0V$ )

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	MM1096A	I <sub>CC</sub>	During watchdog timer operation		100	150	μA
	MM1096B				130	195	
Detection voltage	MM1096A	V <sub>SL</sub>	V <sub>S</sub> =OPEN, V <sub>CC</sub> 	3.10	3.20	3.30	V
	MM1096B			4.05	4.20	4.35	
	MM1096A	V <sub>SH</sub>	V <sub>S</sub> =OPEN, V <sub>CC</sub> 	3.15	3.25	3.35	
	MM1096B			4.15	4.30	4.45	
Detection voltage temperature coefficient		V <sub>S</sub> /ΔT			±0.01		%/°C
Hysteresis voltage	MM1096A	V <sub>HYS</sub>	V <sub>SH</sub> -V <sub>SL</sub> , V <sub>CC</sub> 	25	50	100	mV
	MM1096B			50	100	150	
CK input threshold		V <sub>TH</sub>		0.8	1.2	2	V
CK input current		I <sub>IH</sub>	A : V <sub>CK</sub> =3.6V, B : V <sub>CK</sub> =5.0V		0	1	μA
		I <sub>IL</sub>	V <sub>CK</sub> =0V	-12	-6	-2	
Output voltage (High)	MM1096A	V <sub>OH</sub>	I <sub>RESET</sub> = 1μA	3.0	3.4		V
	MM1096B		V <sub>S</sub> =OPEN	4.0	4.5		
Output voltage (Low)		V <sub>OL1</sub>	I <sub>RESET</sub> = 0.5mA, V <sub>S</sub> =0V		0.2	0.4	V
		V <sub>OL2</sub>	I <sub>RESET</sub> = 1.0mA, V <sub>S</sub> =0V		0.3	0.5	
R output sync current		I <sub>OL</sub>	V <sub>RESET</sub> = 1.0V, V <sub>S</sub> =0V	1	2		mA
C <sub>T</sub> charge current		I <sub>CT1</sub>	V <sub>TC</sub> =1.0V during watchdog timer operation	-0.28	-0.48	-0.96	μA
		I <sub>CT2</sub>	V <sub>TC</sub> =1.0V during power ON reset operation	-1.60	-2.40	-4.80	μA
Minimum operating power supply voltage to ensure RESET		V <sub>CCL</sub>	V <sub>RESET</sub> = 0.4V I <sub>RESET</sub> = 0.1mA		0.8	1.0	V

Products to be discontinued

**Electrical Characteristics (DC)** (Except where noted otherwise, MM1096A :  $V_{CC}=3.6V$ ,  $T_a=25^{\circ}C$ , MM1096B :  $V_{CC}=5.0V$ )  
(Except where noted otherwise, resistance unit is  $\Omega$ )

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub> input pulse width	T <sub>PI</sub>	V <sub>CC</sub> 3.6V 	8			$\mu s$
		V <sub>CC</sub> 2.8V 				
	T <sub>PI</sub>	V <sub>CC</sub> 5.0V 	8			$\mu s$
		V <sub>CC</sub> 4.0V 				
CK input pulse width	T <sub>CKW</sub>	CK  or 	3			$\mu s$
CK input cycle	T <sub>CK</sub>		20			$\mu s$
Watchdog timer monitoring time *1	T <sub>WD</sub>	C <sub>T</sub> =0.02 $\mu$ F	25	50	75	ms
Reset time for watchdog timer *2	T <sub>WR</sub>	C <sub>T</sub> =0.02 $\mu$ F	1	2	3	ms
Reset hold time for power supply rise *3	T <sub>PR</sub>	C <sub>T</sub> =0.02 $\mu$ F, V <sub>CC</sub> 	5	10	15	ms
Output delay time from V <sub>CC</sub> *4	T <sub>PD</sub>	$\overline{RESET}$ pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		2	10	$\mu s$
Output rise time *5	t <sub>R</sub>	$\overline{RESET}$ pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		2.0	4.0	$\mu s$
Output fall time *5	t <sub>F</sub>	$\overline{RESET}$ pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		0.2	1.0	$\mu s$

Notes:

- \*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output. In other words, reset output is output if a clock pulse is not input during this time.
- \*2 Reset time means reset pulse width. However, this does not apply to power ON reset.
- \*3 Reset hold time is the time from when V<sub>CC</sub> exceeds detection voltage (V<sub>SH</sub>) during power ON reset until reset release ( $\overline{RESET}$  output high).
- \*4 Output delay time is the time from when power supply voltage drops below detection voltage (V<sub>SL</sub>) until reset ( $\overline{RESET}$  output low).
- \*5 Voltage range when measuring output rise and fall is 10~90%.
- \*6 Watchdog timer monitoring time (T<sub>WD</sub>), watchdog timer reset time (T<sub>WR</sub>) and reset hold time (T<sub>PR</sub>) during power supply rise can be changed by varying C<sub>T</sub> capacitance. The times are expressed by the following formulae.

$$T_{PR} (ms) \approx 500 \times C_T (\mu F)$$

$$T_{WD} (ms) \approx 2500 \times C_T (\mu F)$$

$$T_{WR} (ms) \approx 100 \times C_T (\mu F)$$

Example : When C<sub>T</sub>=0.02 $\mu$ F

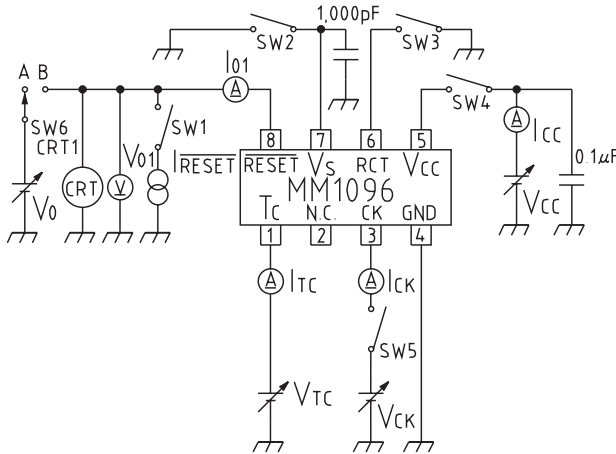
$$T_{PR} \approx 10ms$$

$$T_{WD} \approx 50ms$$

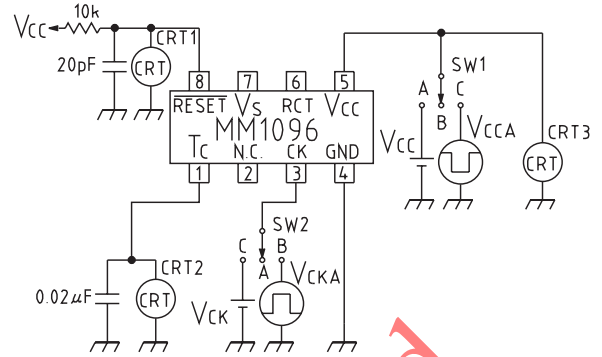
$$T_{WR} \approx 2ms$$

Measuring Circuits

Measuring Circuit 1 (DC)



Measuring Circuit 2 (AC)



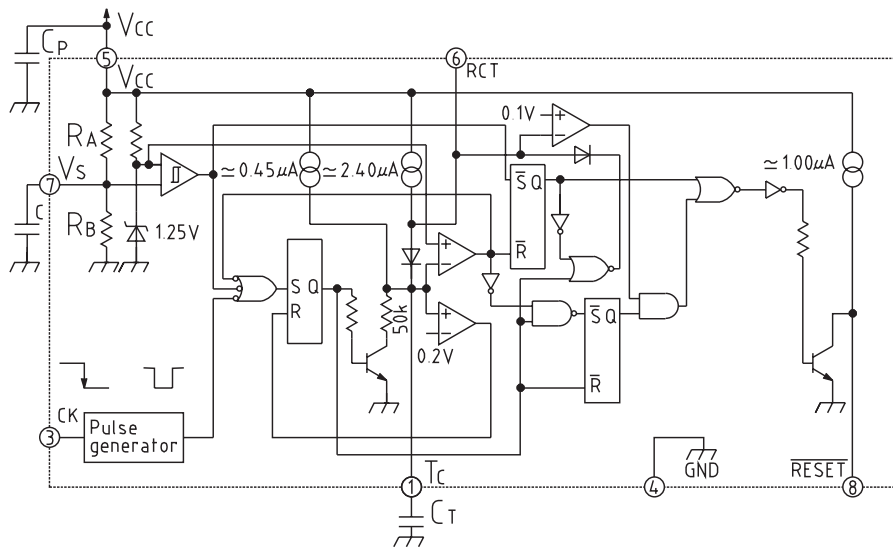
Measuring Circuit 1 SW & Power Supply Table

Item	Symbol	SW1	SW2	SW3	SW4	SW5	SW6	V <sub>CC</sub>	V <sub>CK</sub>	V <sub>CT</sub>	I <sub>RESET</sub>	VM, IM	Notes
Consumption current	I <sub>CC</sub>	OFF	OFF	OFF	ON	ON	A	3.6V	3.6V	0V		I <sub>CC</sub>	
Detection voltage	V <sub>SL</sub>	OFF	OFF	ON	ON	ON	A	3.6V~3V	0V	2V		V <sub>O1</sub> , CRT1	
	V <sub>SH</sub>	OFF	OFF	ON	ON	ON	A	3V~3.6V	0V	2V		V <sub>O1</sub> , CRT1	
CK input threshold	V <sub>TH</sub>	OFF	OFF	OFF	ON	ON	A	3.6V	0V~3V	1V		I <sub>CK</sub> , V <sub>CK</sub>	
CK input current	I <sub>IH</sub>	OFF	OFF	OFF	ON	ON	A	3.6V	3.6V	0V		I <sub>CK</sub>	
	I <sub>IL</sub>	OFF	OFF	OFF	ON	ON	A	3.6V	0V	0V		I <sub>CK</sub>	
Output voltage (High)	V <sub>OH</sub>	ON	OFF	ON	ON	ON	A	3.6V	3.6V	2V	-1μA	V <sub>O1</sub>	
Output voltage (Low)	V <sub>OL1</sub>	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	0.5mA	V <sub>O1</sub>	
	V <sub>OL2</sub>	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	1.0mA	V <sub>O1</sub>	
Output sink current	I <sub>OL1</sub>	OFF	ON	ON	ON	ON	B	3.6V	3.6V	2V		I <sub>O1</sub>	V <sub>O</sub> =1V
C <sub>T</sub> charge current 1	I <sub>Tc1</sub>	OFF	OFF	OFF	ON	OFF	A	3.6V		1V		I <sub>Tc</sub>	
C <sub>T</sub> charge current 2	I <sub>Tc2</sub>	OFF	OFF	OFF	ON	OFF	A	3.6V		1V		I <sub>Tc</sub>	
Minimum operating power supply voltage to ensure RESET	V <sub>CCCL</sub>	ON	OFF	ON	ON	ON	A	0V~2V	0V	0V		V <sub>O1</sub> , V <sub>CC</sub>	

Measuring Circuit 2 SW & Power Supply Table

Item	Symbol	SW1	SW2	V <sub>CCA</sub>	V <sub>CC</sub>	V <sub>CKA</sub>	V <sub>CK</sub>	CRT	Notes
V <sub>CC</sub> input pulse width	T <sub>P1</sub>	C	B		-		-	CRT1 CRT2	T <sub>1</sub> =8μs
CK input pulse width	T <sub>CKW</sub>	A	B	-	3.6V		-	CRT1 CRT2	T <sub>2</sub> =3μs
CK input cycle	T <sub>CK</sub>	A	B	-	3.6V		-	CRT1 CRT2	T <sub>3</sub> =20μs
Watchdog timer monitoring time	T <sub>WD</sub>	A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Reset time for watchdog timer	T <sub>WR</sub>	A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Reset hold time for power supply rise	T <sub>PR</sub>	B→A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Output delay time from V <sub>CC</sub>	T <sub>PD</sub>	C	A		-	-	0V	CRT1	
Output rise time	T <sub>R</sub>	A	A	-	3.6V	-	3.6V	CRT1	
Output fall time	T <sub>F</sub>	A	A	-	3.6V	-	3.6V	CRT1	

Block Diagram



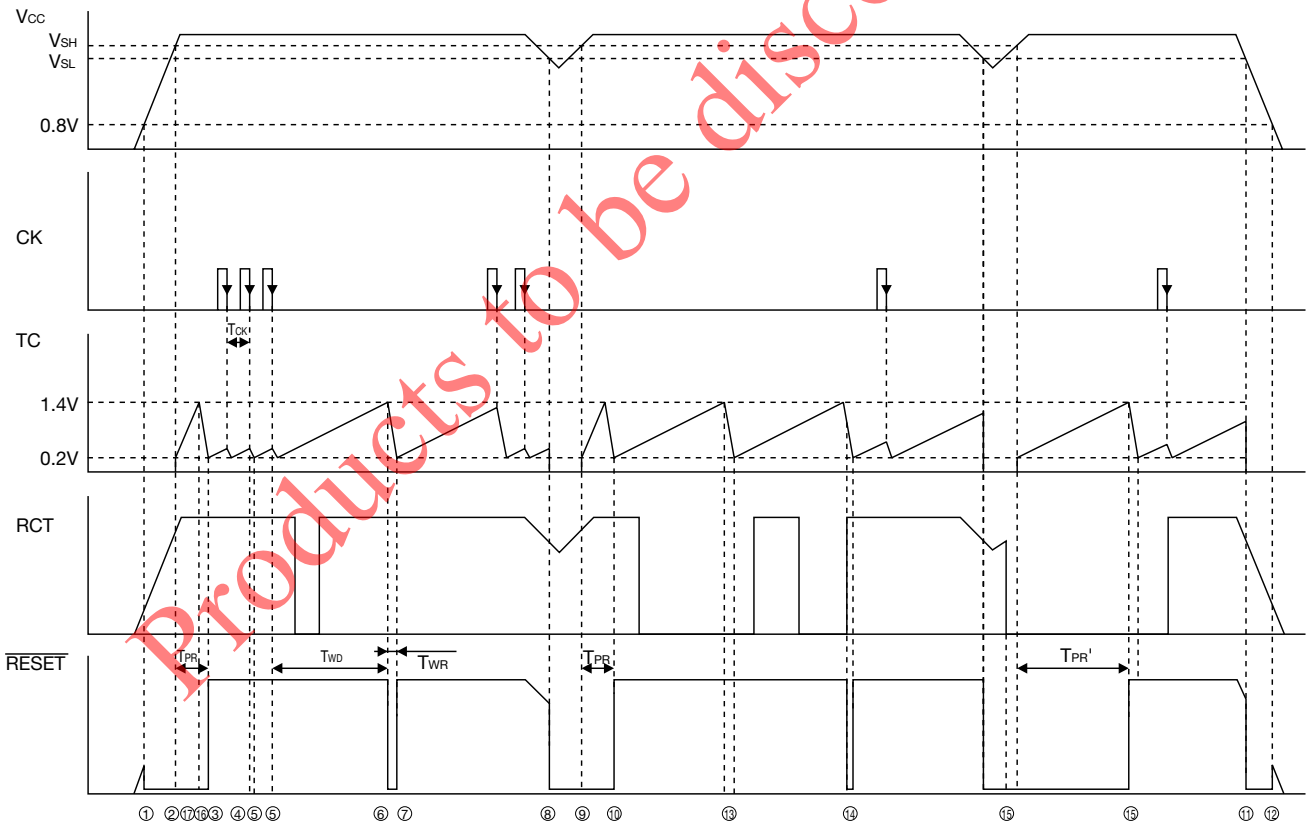
	RA	RB
MM1096A	≈ 305k	≈ 195k
MM1096B	≈ 350k	≈ 150k

Note 1:  $C_P=0.1\mu F$  approx.

Note 2:  $C \geq 1000pF$

Note 3: The watchdog timer can be stopped by connecting the RCT pin to GND. Then it functions as a voltage detection circuit.)

Timing Chart



## Description of Operation

1.  $\overline{\text{RESET}}$  goes low when  $V_{CC}$  rises to approximately 0.8V.  
Approximately  $1\mu\text{A}$  ( $V_{CC}=0.8\text{V}$ ) of pull up current is output from  $\overline{\text{RESET}}$
2. Capacitor  $C_T$  charging starts when  $V_{CC}$  rises to  $V_{SH}$  (MM1096A  $\approx 3.25\text{V}$ , MM1096B  $\approx 4.3\text{V}$ ). Output is in reset state at this time.
3. Output reset is released ( $\overline{\text{RESET}}$  goes high) after a certain time ( $T_{PR}$ ), from when  $C_T$  starts charging until discharge (the time from when  $C_T$  voltage reaches a certain threshold value 1 ( $\approx 1.4\text{V}$ ) until  $C_T$  voltage drops to a certain threshold value 2 ( $\approx 0.2\text{V}$ ).  
Reset hold time :  $T_{PR}$  is as follows.  
 $T_{PR} (\text{ms}) \approx 500 \times C_T (\mu\text{F})$   
 $C_T$  charging starts again after reset release, and watchdog timer operation begins.  
Clock input to the CK pin during  $C_T$  charging will cause mis-operation.
4. If a clock is input (negative edge trigger) to the CK pin during  $C_T$  charging, C switches from charging to discharge.
5. Discharge switches to charging when  $C_T$  voltage drops to a certain threshold value ( $\approx 0.2\text{V}$ ). Steps 4 and 5 are repeated while a normal clock is input from the logic system.
6. Output goes to reset state ( $\overline{\text{RESET}}$  goes low) when the clock ceases and  $C_T$  voltage reaches reset ON threshold value ( $\approx 1.4\text{V}$ ).  
The formula for  $C_T$  charging time ( $T_{WD}$ : watchdog timer monitoring time) until reset is output is as follows.  
 $T_{WD} (\text{ms}) \approx 2500 \times C_T (\mu\text{F})$
7. Watchdog timer reset time  $T_{WR}$  is the discharge time until  $C_T$  voltage drops to reset OFF threshold value ( $\approx 0.2\text{V}$ ). The formula is as follows.  
 $T_{WR} (\text{ms}) \approx 100 \times C_T (\mu\text{F})$   
After reset OFF threshold value is reached, output reset is released and  $C_T$  starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when the clock ceases, 6 and 7 are repeated.
8. Reset is output when  $V_{CC}$  drops to  $V_{SL}$  (MM1096A  $\approx 3.2\text{V}$ , MM1096B  $\approx 4.2\text{V}$ ).  $C_T$  is charged simultaneously.
9.  $C_T$  charging starts when  $V_{CC}$  rises to  $V_{SH}$ .  
When  $V_{CC}$  drops momentarily,  $C_T$  charging begins after the charge is first discharged, if the time from  $V_{CC}$  dropping below  $V_{SL}$  until it rises to  $V_{SH}$  is longer than the  $V_{CC}$  input pulse width standard value  $T_{PI}$ .
10. Output reset is released after  $V_{CC}$  goes above  $V_{SH}$  and after  $T_{PR}$ , and the watchdog timer starts. Thereafter, 8~10 are repeated when  $V_{CC}$  goes below  $V_{SL}$ .
11. When power is OFF, reset is output if  $V_{CC}$  goes below  $V_{SL}$ .
12. When  $V_{CC}$  drops to 0V, reset output is held until  $V_{CC}$  reaches 0.8V.
13. Output of the reset pulse stops if RCT pin goes "LOW".
14. TC pin keeps charging/discharging even if RCT pin goes "LOW". Therefore if RCT is release and  $C_T$  is discharged at the same time, output goes "LOW" when RCT release. To avoid this operation, input CK before the  $T_{WR}$  time of RCT release and discharge  $C_T$ .
15. RESET output is released after the power on time in case of startup with RCT pin "LOW". (Operating as a reset with power on reset) The power on reset time is as follows:  
 $T_{PR}' \approx T_{WD} - T_{WR} \approx 2400 \times C_T (\mu\text{F})$
16. There might be low pluse in output at the  $C_T$  switching point from charging to discharging during power on reset at low temperature. If low pluse of reset output is a problem in operation, add capacitance  $C_{OUT}$  between  $\overline{\text{RESET}}$  - GND. Recommended value is as follows:  
 $C_{OUT} (\mu\text{F}) > 10^4 \times C_T (\mu\text{F}) / R_L (\Omega)$
17. RESET output keeps "LOW" if CK is input during  $T_{PR}$ . RESET output goes "HIGH" once CK is released. Noise jumps into CK easily if CK output of microcomputer is high impedance during  $T_{PR}$ . Pull down a resistance (approx. 10-100k $\Omega$ ) to CK pin and lower the impedance or keep the IC away from noise if there's a possibility of defects such as RESET output keeps "LOW" due to CK malfunction caused by noise.